INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)

e-ISSN : 2583-1062

Impact Factor : 5.725

www.ijprems.com
editor@ijprems.com

Vol. 03, Issue 09, September 2023, pp : 424-427

A NOVEL DESIGN OF 1 BIT ADDER USING (5T) GDI TECHNIQUE

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ABSTRACT

Addition is a basic mathematical procedure that is used to calculate addresses, table indices, and other related tasks. It serves as the foundation for an arithmetic operation and is used in processors and VLSI (Very Large Scale Integration) (ASICs). The two key factors that should be taken into account in digital circuits are speed and power dissipation. To achieve greater performance than adders previously built using other methods, a design for a 1-bit adder utilizing the GDI (Gate Diffusion Input) approach using only 5 transistorsis suggested. Tools used for stimulation are DSCH & MICROWIND.

Keywords: VLSI, GDI, CMOS, W-width, Y-output, A,B-input, L-logiclow, H-logichigh

1. INTRODUCTION

The most crucial factors for digital circuit designers nowadays are fast speed, high throughput, minimal silicon area, and low power consumption of digital circuits. All digital circuits are constructed using logic gates. Moreover, circuits for doing math frequently use1-bit adder cells.ALU, CPU, and floating point devices all frequently use adders. Basic adders include half and full adders. For the most part, CMOS logic is used to create these circuits. Here, we present cutting-edge GDI-based architecture for a 1-bit half-adder. The GDI technique enables the execution of numerous sophisticated logic operations by using two transistors. In terms of latency, power usage and area (number of Transistors), GDI logic performs better than CMOS logic.

2. METHODOLOGY

GDI TECHNIQUE

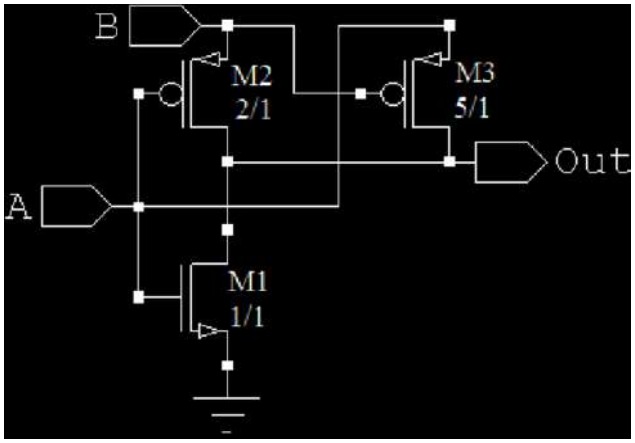
In low-power applications, the GDI method has taken the place of the CMOS method, reducing latency, size, and power consumption. It has two N-inputs for the NMOS source and drain and one P-input for the PMOS source and drain, making three inputs shared by the PMOS and NMOS gates. The N, P, and G terminals in GDI can accept a supply of VDD, are grounded, or a specified input signal

3. ADVANTAGES OF GDI OVER OTHER TECHNOLOGY

- Design of low-power circuits
- Enables lowering energy usage.
- Shortening the propagation lag.
- Making the digital circuit smaller
- Keeping the complexity of the logic design low

3T XOR GATE

A modified CMOS inverter and a PMOS pass transistor make up the design. When input B is at logic high, the inverter behaves like a standard CMOS inverter, and the pass transistor M3 receives the same logic value as input A. However, when AB = 00, a threshold drop occurs, which can be lessened by increasing the W of M3, which causes the output Y to decrease in respect to the input. Due to a threshold drop over M3, the output becomes worse for AB=10.



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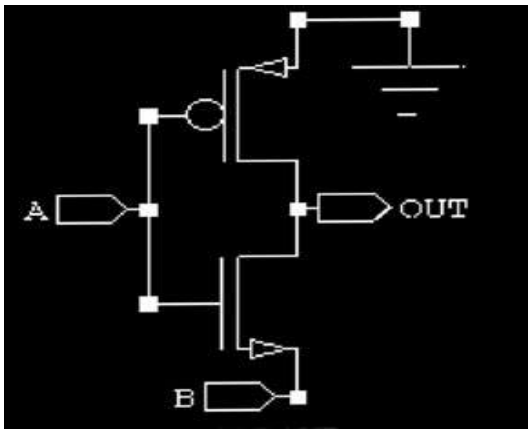
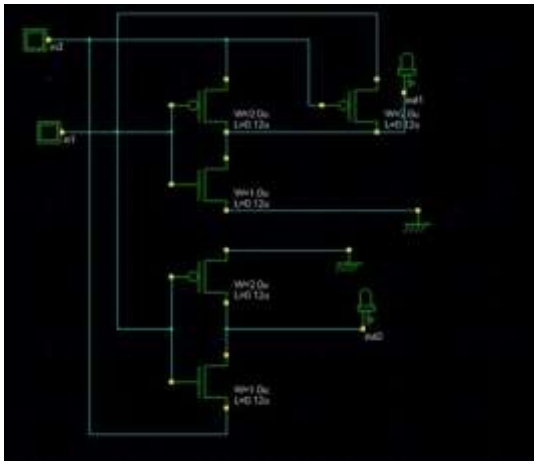
2T AND GATE

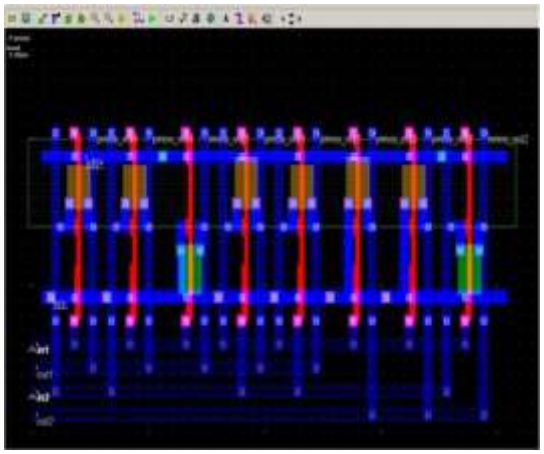
The PMOS transistoris ON and the NMOS transistor is OFF when AB = 00 and 01, respectively, in the modified GDI AND gate. The NMOS transistor provides an incomplete logic high signal when AB= 11, while the PMOS transistors ends a completelogic low signal when AB = 10. This is due to the DIBL effect, which causes NMOS to experience sub-threshold current flow, which has an impact on the output.



DESIGN OF 1- BIT HALF ADDER USING (5T)GDI TECHNIQUE



DESIGN LAYOUT OF 1-BIT HALF ADDER USING (5T) GDI TECHNIQUE



4. RESULTS AND DISCUSSIONS PROCEDURE

Step1: Draw the proposed design of 1-bit half adder in DSCH and save the schematic with. SCH extension.
Step2: Check the functionality with the help of the functionality table.
Step3: Now click start stimulation and give the input vectors and verify the output.
Step4: Conver the schematic into Verilog file and save it with the. txtextension.
Step5: Open MICROWIND and compile the Verilogfile.
Step6: Click back to the editor to view the design layout and save it with the. MSK extension. Step7: Now click start stimulation and measure the delay between input and output.

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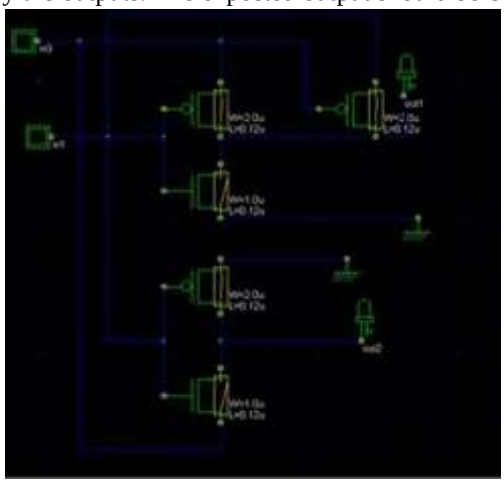
5. FUNCTIONALVERIFICATION

The functionality of the designed 1bit half adder is verified by giving patterns. The vectors are mentioned in the table given below

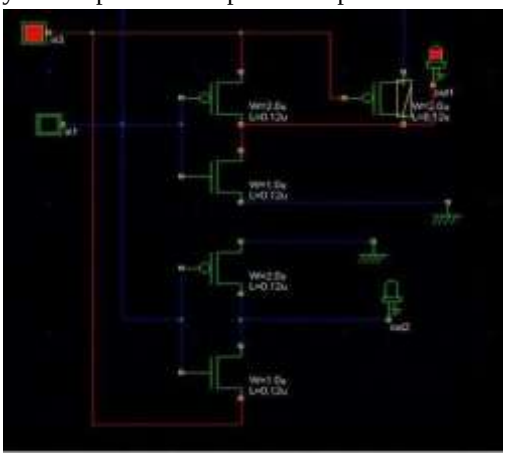
HALF ADDER TRUTH TABLE FOR FUNCTIONALVERIFICATION

I/P- A	I/P- B	O/P- S	O/P- C
0 (L)	0 (L)	0 (L)	0 (L)
0 (L)	1 (H)	1 (H)	0 (L)
1 (H)	0 (L)	1 (H)	0 (L)
1 (H)	1 (H)	0 (L)	1 (H)

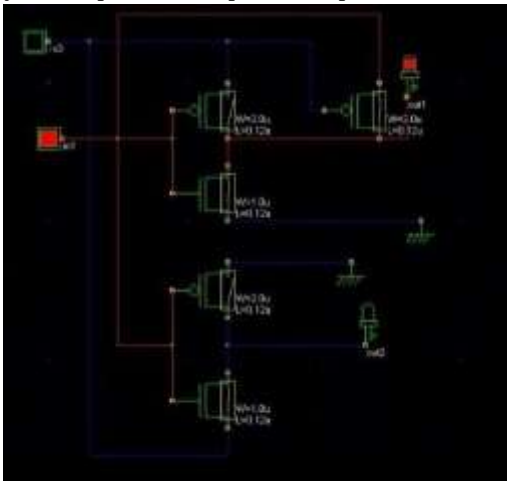
Apply Input A=0 and B=0 and verify the outputs. The expected output should be S=0 and C=0



Apply Input A=0 and B=1 and verify the outputs. The expected output should be S=1and C=0



Apply Input A=1 and B=0 and verify the outputs. The expected output should be S=1 and C=0



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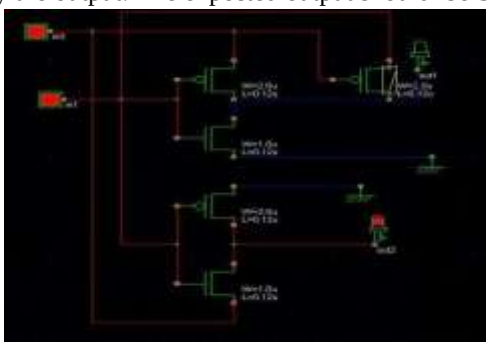
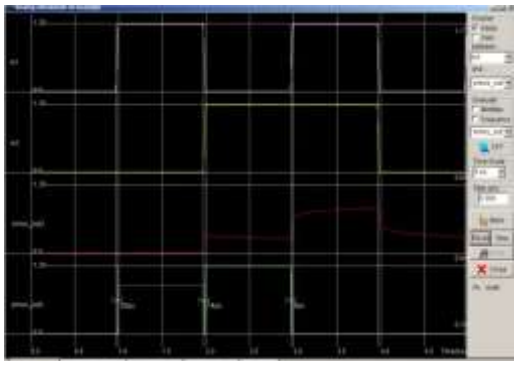
Apply Input A=1 and B=1 and verify the output. The expected output should be S=0 and C=1



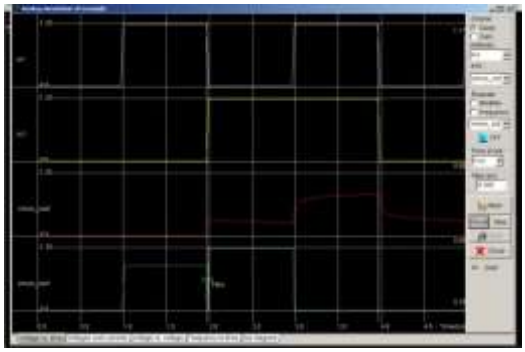
6. TIMING PARAMETERS

The voltage Vs time graph is plotted for both sum (p-mos out) and the carry (n-mos out).The delay between input A and sum and the delay between input B and sum is visualized. From this the rise time delay and the fall time delay are calculated. The decrease in the number of delay increases the speed of the circuit The time scale used for the stimulation is 5ns

DELAY BETWEEN INPUT A AND PMOS OUT



DELAY BETWEEN INPUT B AND PMOS OUT



7. CONCLUSION

A novel 1-bit half-adder design has been successfully developed, and its timing and functional parameters have been confirmed. The speed is raised, and the latency, area, and power dissipation are decreased as a result of using fewer transistors. A novel method for creating a low power half adder with GDI cells is suggested. This one-bit half-adder is created with variously configured GDI cells, resulting in little power consumption due to the low transistor count. It can be used as a building block for programmes that utilize arithmetic logic units (ALUs) and digital signal processing. DSCH and the MICROWIND 3.1 simulator are used to do the analysis and simulation.

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