

A REVIEW OF FAULT DIAGNOSIS FOR VLSI CIRCUITS BASED ON MACHINE LEARNING ALGORITHMS

Dr. V. Jayapradha¹

¹Assistant Professor, Department of ECE, SCSVMV Deemed to be University

ABSTRACT

Testing of Circuits in the VLSI design is the most complicated and vital process. Hence it requires automated working algorithms to detect the faults in the circuit. Machine learning is a set of algorithms that works on learning data from the past. This paper discusses the overview of machine learning algorithms for fault detection in VLSI Circuits.

Keywords: ATPG, Bscan, Stuck-at-faults, SVM, and PCA.

1. INTRODUCTION

A circuit that is solely defined by a logic-level network list (schematic) is tested using patterns created automatically using a method known as automatic test-pattern generation (ATPG). These procedures typically use a fault generator to generate the smallest possible collapsed fault list, freeing the designer from having to worry about fault generation. In a sense, ATPG algorithms serve several purposes because they can produce circuit test patterns, identify redundant or unneeded circuit logic, and establish whether one circuit implementation is identical to another.

Faults are more likely to occur on the circuit because the variety of transistors on the circuit is greatly expanding, especially for large-scale circuits [7]. Therefore, check patterns should be used to thoroughly inspect the circuit's practicality. A stuck-at-fault is a fault model that is frequently employed at the gate level to account for the benefit of check generation.

2. STUCK-AT-FAULT

The stuck-at-low and stuck-at-high tests are the two faults that make up the stuck-at test. For the stuck-at-low test, one or more test steps will be generated.

If at all possible, each test step has a high level for all BScan nets [6]. By separating the stuck-at test from the test for shorts, it is possible to clearly identify the different error types. Each drivable pin drives a high level at least once in the stuck-at-low part, and each input and the bidirectional pin measures a high level at least once (real stuck-at test).

For the purpose of identifying stuck-at faults in 27-channel interrupt controller, ALUs circuits from ISCAS'85 benchmarks, a novel fault detection method based on an artificial neural network is proposed in this study [1]. The suggested algorithm makes an effort to avoid the search space explosion problem by compressing features of digital circuits. The proposed SSAE has connected with SoftMax classifier as a last hidden layer for carrying out the supervised learning phase using the fault mask for each test pattern generated from the ATALANTA tool. On eight combinational circuits from ISCAS'85, the suggested methodology has been applied. With the help of the ATALANTA tool, the maximum fault coverage is delivered at 99.3%. Additionally, for eight combinational circuits, the SSAE network achieves a maximum validation accuracy of 99.7% through feature-reducing test patterns.

This research presents [2] one type of random forests-based fault diagnosis approach for power electronics and the goal is to examine different design ideas and see how successfully random forests diagnose faults in power electronic circuits. The best random forest configurations are discovered through experimental research. The procedure is workable and efficient, according to experimental data. This diagnostic technique has a wide range of applications and can also be applied to other circuit types.

This paper [3] addressed fault diagnosis for cascaded H-bridge multilevel inverter systems. A PCA-mRVM (principal component analysis multi-class relevance vector machine)-based fault diagnosis approach has been suggested in this situation. The following are the key goals of this strategy: Signal pre-processing based on FFT identifies some distinguishing characteristics; dimension reduction based on PCA increases fault detection effectiveness; and mRVM, which outputs classification findings as binary codes, improves diagnosis accuracy. The obtained findings clearly demonstrate the suggested PCA-mRVM fault diagnostic strategy's superiority to conventional techniques when compared to PCA-BP and PCA-SVM.

The majority of these models concentrate on acquiring a circuit's output response to a test pattern; various pre-processing techniques are used, and this data is then applied as input to the ML model, which aims to categorize the defect. In [4], the two-layer MLP used to find the problem is fed the Fourier harmonic components of the CUT response, which are simulated from a sinusoidal input signal. Additionally, a NN is given input using a selection criterion for choosing the optimal components to characterize the behavior of the circuit in fault-free (nominal) and fault circumstances [5]. The NN organizes the faults into a fault dictionary together with clustering.

3. CONCLUSION

This paper discusses the ML-based defect analysis for industrial standards, it has revolutionized the speed and precision of automatic defect categorization, which has been around for a while. Automated defect analysis must receive a lot of attention if the source of the defect is to be found.

4. REFERENCES

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