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DESIGN AND VERIFICATION OF 4-BIT SHIFT REGISTERS IN GPDK-45NM TECHNOLOGY

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ABSTRACT

This paper details the design, implementation, and verification of four fundamental 4-bit shift registers configuration Serial-In Serial-Out (SISO), Serial-In Parallel-Out (SIPO), Parallel-In Serial-Out (PISO), and Parallel-In Parallel-Out (PIPO). These are implemented by using Transmission Gate (TG)–based flip-flop structures in the GPDK 45 nm CMOS technology. Shift registers serve as critical sequential building blocks for data storage, buffering, and communication interfaces in digital systems. The primary work involves establishing optimized transistor-level schematics, analyzing their performance metrics (such as delay and power consumption), and verifying the physical design using industry-standard flows. The schematic-level designs utilized TG-based latches to achieve superior low-power and high-speed behavior. Post-implementation verification, including Design Rule Check (DRC) and Layout Versus Schematic (LVS), confirmed the fidelity of the physical design. The final results demonstrate that the TG based implementations in the 45 nm process achieve efficient operation with reduced leakage and improved switching characteristics, confirming their suitability for modern high-speed and low-power digital systems.

Keywords: Shift Register, CMOS, 45 nm, Transmission Gate (TG), VLSI, SISO, SIPO, PISO, PIPO.

1. INTRODUCTION

Shift registers are essential components of sequential logic circuits, utilized ubiquitously for temporary data storage, serial-to-parallel, and parallel-to-serial data conversion. The core functionality relies on a cascade of flip-flops (FFs) that synchronize the shifting of digital data. This work addresses four standard configurations:

Serial-In Serial-Out (SISO): Data input and output are sequential,

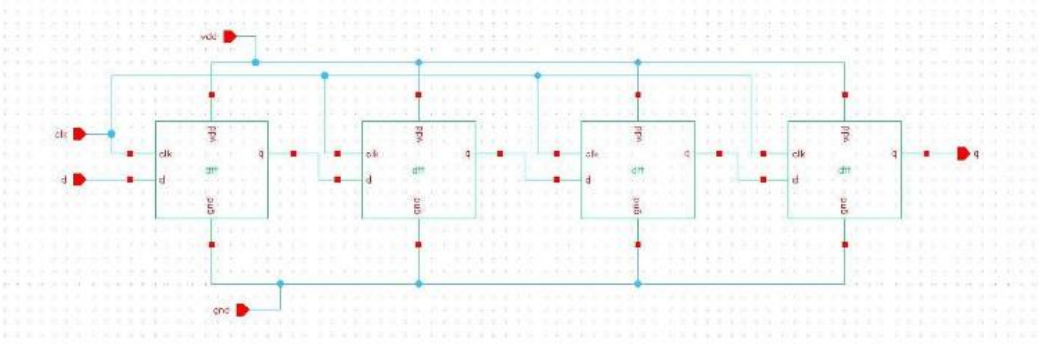

Fig (1): Schematic Diagram of 4-bit Serial-In Serial-Out (SISO) Register

Serial-In Parallel-Out (SIPO): Data input is sequential, and output is parallel.

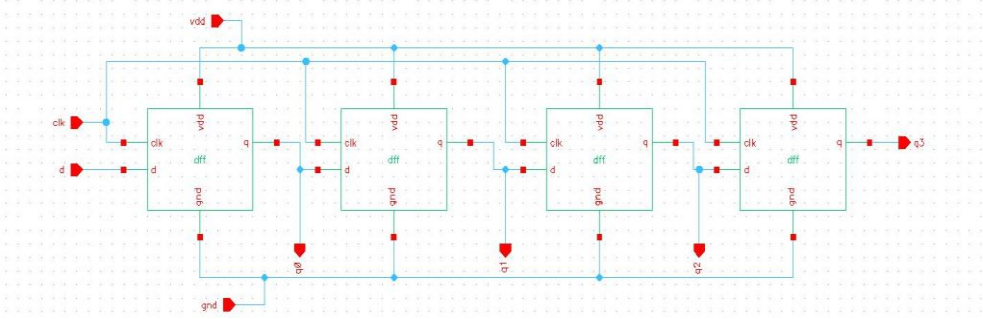

Fig (2): Schematic Diagram of 4-bit Serial-In Parallel-Out (SIPO) Register

Parallel-In Serial-Out (PISO): Data input is parallel, and output is sequential.

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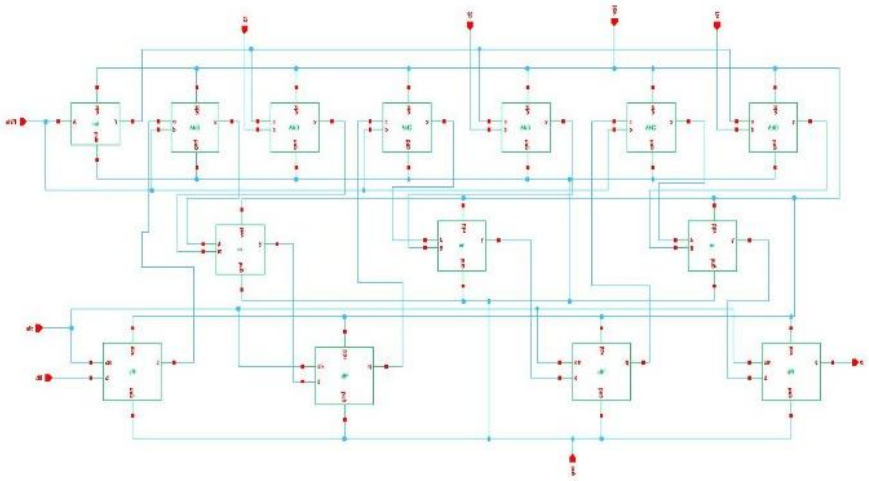

Fig (3): Schematic Diagram of 4-bit Parallel-In Serial-Out (PISO)Register

Parallel-In Parallel-Out (PIPO): Data input and output are both parallel.

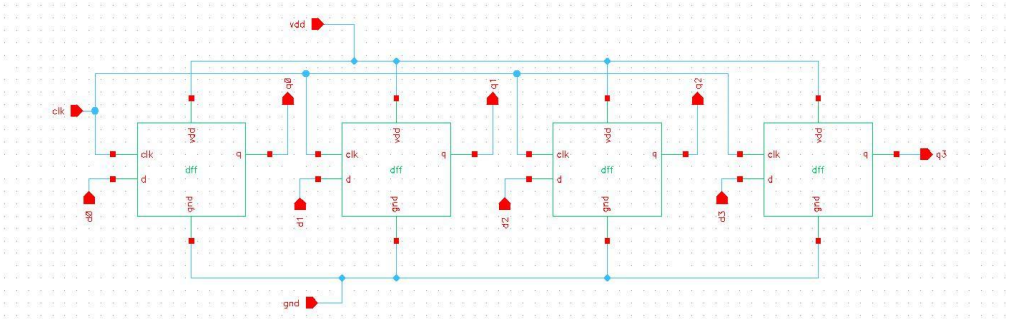

Fig (4): Schematic Diagram of 4-bit Parallel-In Parallel-Out (PIPO)Register

The motivation for this project was to leverage advanced semiconductor technology and optimized circuit design to achieve high-performance operation. Specifically, this paper focuses on utilizing the GPDK 45 nm CMOS technology and implementing Transmission Gate (TG)-based flip-flops known for their efficiency and compact size to design the four 4-bit shift register architectures. The implementation was verified through a complete VLSI design flow, from schematic capture to physical verification.

2. LITERATURE SURVEY

1. Modern Shift Register Design (2017)

The recent research is all about making shift registers faster and less power-hungry by designing better alternatives to standard flip-flops:

Implementations using Pulse Latches (Chavhan & Thakare, 2017): This paper introduced pulsed latches (specifically SSASPL on 180nm CMOS) as a compact, low-power replacement for flip-flops. The result was better timing and a smaller load on the clock for high-speed uses.

Performance Evaluation (Sengupta & Dastidar, 2017): This study created a low-power 4-bit Universal Shift Register by combining pulsed latches with clock gating (on 90nm CMOS). This clever technique drastically cut down on power use and switching, which is perfect for battery-powered or portable gadgets.

2. The Essential Foundations (2008 & 2015)

To do this advanced chip design, you need a strong technical base, which these books provide:

Digital System Design using VHDL (Roth & Kurian, 2008): This text covers how to model and simulate digital systems using VHDL, giving you the necessary architecture and design skills.

Digital Circuits and Design (Kothari & Dhillon, 2015): This book teaches a practical modular circuit design method based on VHDL, supported by real-world examples for efficient system building and testing.

3. METHODOLOGY AND ARCHITECTURE

A. VLSI Design Flow

The project follows a standard VLSI design flow, starting with schematic entry and functional simulation, and then towards the layout design, and concluding with physical verification. The specific design steps included:

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- Schematic Entry and Simulation
- Layout Design
- Design Rule Check (DRC)
- Layout Versus Schematic (LVS) verification

B. Core Storage Element

The fundamental building block used in all four register configurations is the Transmission Gate (TG)based flip-flop. The TG-based latches were selected to specifically target low-power and high-speed behavior due to their strong switching characteristics and minimal static power dissipation compared to fully static CMOS designs.

C. Shift Register Configurations

Each of the four 4-bit shift registers (SISO, SIPO, PISO, and PIPO) was constructed by cascading and interconnecting four TG-based D Flip-flops. The specific interconnection logic (e.g., control logic for PISO/PIPO parallel loading) was optimized to ensure efficient data handling for each respective architecture.

4. RESULTS AND ANALYSIS

A. Functional and Physical Verification

Functional verification was performed by simulating each shift register architecture under input sequences and clock conditions to verify the needed data loading and shifting operations.

Post-layout verification confirmed the manufacturing readiness of the physical designs:

Design Rule Check (DRC): Performed to confirm the layouts complied with the geometric constraints of the 45 nm fabrication process.

Layout Versus Schematic (LVS): This is performed so as to ensure that the transistor-level connectivity of the physical layout was an accurate representation of the original schematic design.

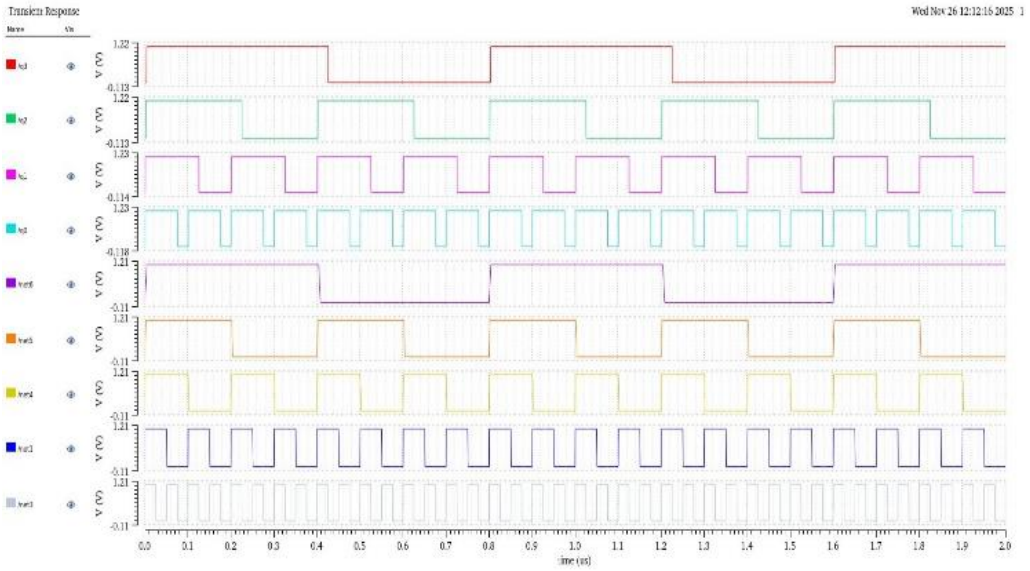

Fig (5): Transient Response of 4-bit shift register

B. Performance Analysis

Extensive performance analysis was done on all four shift register configurations. While specific numerical data (Power/Delay/PDP/EDP) were calculated, the qualitative results confirm the following:

Low Power Consumption: The TG-based flip-flop structures contributed significantly to achieving low power consumption in all four designs.

Reduced Propagation Delay: The use of 45 nm CMOS technology ensured a high-speed design with a reduced propagation delay.

Operational Efficiency: The TG-based implementations achieved reduced leakage and improved switching characteristics when compared to traditional structures.

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Table 1: Performance Parameters of the 4-bit Shift Registers

SL.NO	Logic Gate	Transistor count	Average Power for 1.1 volt (uW)	Average Delay	Area (um^2)
1.	4-bit SISO	72	14.98E	459.2ps	827.17
2.	4-bit SIPO	72	14.98E	463.68ps	944.15
3.	4-bit PISO	128	28.79E	91.71ps	1405.33
4.	4-bit PIPO	72	26.51E	440.41ps	742.79

C. Data Handling Characteristics

The analysis highlighted performance differences between the configurations based on data handling:

SISO and SIPO configurations demonstrated sequential data movement, making them ideal for simple serial communication applications.

PISO and PIPO setups enabled quicker data movement and simultaneous parallel loading, which made them ideal for applications requiring high throughput.

5. CONCLUSION

The design, simulation, and verification of the 4-bit SISO, SIPO, PISO, and PIPO shift registers using Transmission Gate flip-flops in 45 nm CMOS technology successfully met all project objectives. The results conclusively show that all four configurations operate correctly and are highly optimized for performance. Employing the 45 nm technology node along with the TG-based architecture provided key benefits, such as lower power usage, shorter propagation delays, and a compact layout footprint. The thorough physical verification steps (DRC and LVS) additionally validate that the design is both manufacturable and functionally accurate. Overall, these shift-register implementations demonstrate strong efficiency and reliability, making them highly suitable for incorporation into contemporary high-speed, low-power digital systems.

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