

ELECTRICAL CHARACTERISTICS ANALYSIS OF DOUBLE GATE TUNNEL FETS FOR MODERN ICS

Murugan¹, Jegan M², Manoj S K³, Dr. T. S. Arun Samuel⁴

^{1,2,3}B. E, ECE, National Engineering College, Kovilpatti, India.

⁴Professor, ECE, National Engineering College, Kovilpatti, India.

ABSTRACT

Complementary metal oxide semiconductor (CMOS) technology has advanced so rapidly over the previous three decades that no one in developed nations can now survive without it. In place of traditional MOS transistors, modern integrated circuits (ICs) use FinFET. Short channel lengths were necessary and are now practicable to achieve quicker speeds and greater package densities. Leakage currents and other undesirable effects have recently been linked to short channel lengths. The thickness of the gate oxide is scaled in proportion to channel length (L) and breadth to prevent the short channel effect (SCE) and maintain a constant electric field in the oxide. By using a Double Gate (DG) TFET transistor, the proposed approach replaces the FinFET prevalent in modern technology.

1. INTRODUCTION

There is an increasing need for smaller, low-power microelectronics due to the present surge in smartphones and tablet computers. Modern CPU and memory storage device generations are particularly significant. These new technologies must meet extremely challenging standards, like being quick and effective while also being more powerful and able to store more data, as well as being physically small, reasonably priced, and dependable. Moore's Law is a well-liked theory that's fueling this trend. Every two years, a microchip's transistor count doubles in accordance with Moore's Law. According to the law, we can anticipate a two-year rise in the speed and functionality of our computers while still paying less for them. Nanoscale design and fabrication are required for such tiny devices. At this scale, atomic scale processes become crucial, and it is vital to comprehend how individual atoms and electrons move inside the materials. Little changes can have a significant influence on the endurance and performance of a device. In general, there are two methods for scaling that may be used. The first is to advance existing technologies by utilizing superior production techniques and materials. The second is to create new technologies that serve the same purpose as the old ones, such as storing memory, but do it on a chip with a higher density.

2. OBJECTIVE

By shrinking transistor sizes, the project's main goal is to create high-speed devices. Since power dissipation must be reduced as technology scales, portable electronics' batteries last longer. The subthreshold gate control of multi-gate MOSFET architectures (double-gate, triple-gate, and gate-all-around MOSFETs) constructed on SOI wafers is superior to that of ordinary MOSFETs. Thermal limitation, which precludes subthreshold performance at low drain voltage, restricts how small MOSFET layouts may go. In MOSFETs, charge carriers are thermally injected across the barrier, whereas in TFETs, charge carriers are injected by gate field-driven band-to-band tunnelling (BTBT) from the source to the channel. Carrier tunnelling is prevented and the leakage current is kept to a minimum in the OFF state thanks to the absence of alignment between the valence band of the source and the conduction band of the channel. But in the ON state, the gate field causes the channel region's conduction band to be dragged down, allowing it to line up with the source region's valence band. This alignment enables charge carrier injection and tunnelling from the source region by lowering the tunnelling barrier's breadth and height. With a threshold of 60 mV/dec, TFET devices can therefore operate much below sub-thermal limits. When the bands are in alignment, this enables rapid turn-on. Due to the TFET's comparatively high barrier to minority carriers, injection of minority carriers yields low leakage current in the OFF state.

3. LITERATURE SURVEY

SURVEY- 1

Using a compact direct current modelling technique (TFETs), the band-to-band tunnelling current in double-gate tunnelling effect transistors is calculated in this study. The physical model equations are solved in closed form by integrating 2-D effects and are then implemented in the Verilog-A hardware description language. Two stages of model verification are carried out. First, the modelling approach is validated using data from the band diagram, transmission current, output current characteristics, and output conductance of the TCAD Sentaurus simulation. High concordance between modelling findings and TCAD data is shown.

The model is subsequently verified using data collected from complementary nanowire gate all-around TFET devices,

which also identifies possible application domains. In the process of verifying, the benefits and drawbacks are examined and resolved. The model's numerical stability and adaptability are demonstrated through simulation of a single-stage TFET inverter.

SURVEY – 2

An analytical charge-based model for the intrinsic capacitances of tunnel field-effect transistors (TFETs) is presented in this paper. The model, which was developed for a-Si double-gate (DG) n-TFETs, is versatile enough to be used to single-gate or p-type TFETs as well. Data from measurements and TCAD simulations are compared to validate the model. There are a number of inconsistencies between TCAD simulations, compact models, and measurements when it comes to the capacitance of planar p-type TFETs manufactured of Si that are constructed on ultrathin bodies. Here, an explanation is established by examining the impact of the Schottky barrier NiSi₂ contacts on the associated differences and the unexpected behaviour of the intrinsic capacitances. There is also a description of how to incorporate this impact into the previous model.

SURVEY - 3

The impact of ambipolarity and trap-assisted tunneling (TAT) on the DC and transient behavior of tunnel field-effect transistors (TFETs) are examined in this work using a straightforward model. The model written in the Verilog-A programming language represents both the AC and DC characteristics of the TFET. The tiny numerical model's adaptability and robustness enable the modeling of the TFET both at the circuit level and as a standalone component. As a result, it is utilized to simulate both a TFET inverter and a 3-stage TFET ring oscillator. The impacts of TAT and TFET ambipolarity are assessed using simulations for various trap densities and drain doping levels.

SURVEY – 4

The main challenges are SS60 mV/dec experimental detection, high ON currents, and resolving the ambipolar behaviour of tunnel FETs. The experimental demonstration of a double-gate, strained-ge, heterostructure tunnelling FET (TFET) with SS60 mV/dec and extraordinarily large driving currents. The record-breaking drive current of 300 $\mu\text{A}/\mu\text{m}$ (the highest ever recorded experimentally for a TFET) and the subthreshold slope of 50 mV/dec were produced by the electrostatics of the DG structure and the narrow bandgap of s-Ge. In order to address the ambipolar problem and look into the scalability of TFETs (direct and phonon-assisted), we have also constructed a thorough TFET simulator that combines a quantum transport model, non-local BTBT, full band structure (real and complex) information, and incorporates all transitions. With the aid of this simulator, we have looked at the scalability of three asymmetric DG TFET designs (underlapped drain, reduced drain doping, and lateral heterostructure). In doing so, we looked into their capacity to produce high ON and low OFF currents as well as resolve ambipolar behaviour.

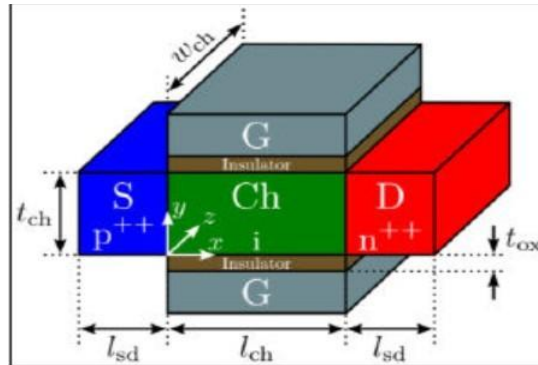
SURVEY – 5

In this study, we construct a simple capacitance model for double-gate TFETs. To support the construction of the model, capacitance voltage measurements were performed on all-silicon SOI TFETs under different biasing methods. The model was validated using DG-TFET simulations performed with TCAD. The proposed model can be used for SPICE modeling of TFETs since no fitting parameters or iterative procedure are used in the development of the model. The model provides a physical perspective for evaluating the transient performance of TFET-based circuits. TCAD simulation results agree well with the proposed model. The model is verified for various structural and bias parameters.

4. PROPOSED SOLUTION

Continuous scaling of MOSFETs encounters a number of difficulties, such as the short-channel effect in which current is generated in the OFF state as the channel length decreases, resulting in significant leakage current and high power dissipation, and limiting the sub-threshold swing (SS) to 60 mV/decade. New MOS devices must be developed to continue scaling to reduce these limitations in MOSFETs. One possible alternative to the traditional MOSFET is the tunnel field-effect transistor (TFET). In this study, an overview of tunnel field effect transistor (TFET) is presented to reduce the limitations and difficulties of traditional MOSFET technology. Different TFET architectures with different doping levels and materials are investigated to improve the device functionality. The high ON state current, low ambipolar current, low SS and low threshold voltage of the TFET make it suitable for analogue applications as well as high frequency applications.

DIAGRAM

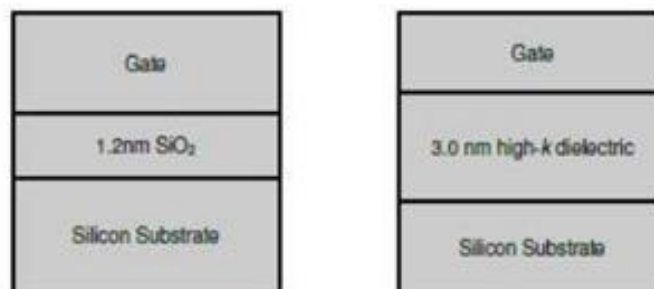


DOUBLE GATE TFET:

A double-gate TFET consists of two gates, one of which is at the top and is called the front gate (also called the back gate). Since the field lines from the gate now terminate at the back gate rather than in the channel, this arrangement improves the electrostatic control of the gate on the channel. Since there are two channels where a larger amount of current can flow through the device, the ON state current is also larger compared to a single gate TFET (SG-TFET). Double Gate P-Channel TFET (DG) Schematic Applying two gate voltages doubles the current in double gate tunnel FETs. The ON current is therefore higher than in a single-gate TFET. OFF -current is less intense. At various V_{ds} voltages and I_{off} , the efficiency of TFETs decreases. This is a commendable achievement in energy saving for low power devices compared to MOSFET.

HIGH DIELECTRIC MATERIAL

In contrast to silicon dioxide, a "high k dielectric material" is a substance with a high dielectric constant k .



In semiconductor fabrication, high-k dielectrics are often used to replace a silicon dioxide gate dielectric or other dielectric material to increase the ON current of the device. Silicon dioxide (SiO_2) has been used as a gate oxide material for many years. The thickness of the silicon dioxide gate dielectric has steadily decreased as transistors have become smaller, increasing the gate capacitance and thus the drive current and improving device performance. Nevertheless, the higher gate capacitance leads to an increase in leakage current. Leakage currents from tunneling increase dramatically when the thickness drops below 2 nm, resulting in increased power consumption and decreased device reliability. ON These dielectrics provide a solution to the low current problem encountered in existing tunneling FETs by reducing the thickness of the gate oxide.

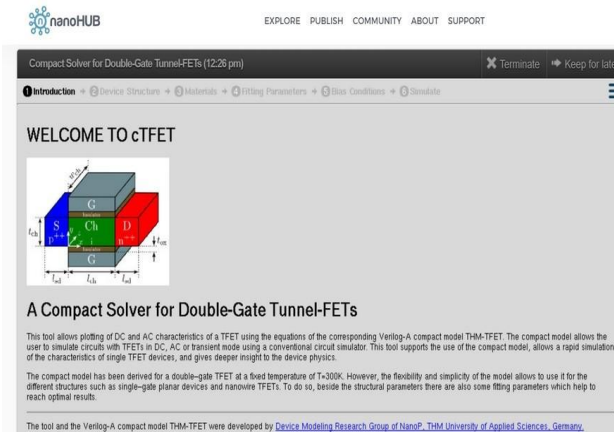
1. SIMULATOR TOOL

The leading open and free platform for computational research, instruction, and cooperation in the domains of nanotechnology, materials science, and related disciplines is Nanohub.org. Using the equations of the appropriate Verilog-A compact model THM- TFET, this feature lets the display of a TFET's output and transfer characteristics. With the help of the miniature model, users may simulate TFET-based circuits in DC, AC, or transient modes using a regular circuit simulator. This tool facilitates the use of the compact model, enables quick modeling of the properties of single TFET devices, and provides a more comprehensive understanding of device physics.

COMPACT SOLVER FOR DOUBLE-GATE TUNNEL-FET

This simulator programme can be found at nanohub.org. We will use this simulator to study our TFET and see how different material factors (such as dielectric constant) and changing voltages affect the output and transmission characteristics.

SIMULATION INTERFACE



Five distinct options are offered in the simulator to replicate the desired output result. To get the outcome, we must mention the following factors:

- Device Component Materials adjusting the settings.
- Condition of bias (V_{gs} , V_{ds} values)
- Simulate.

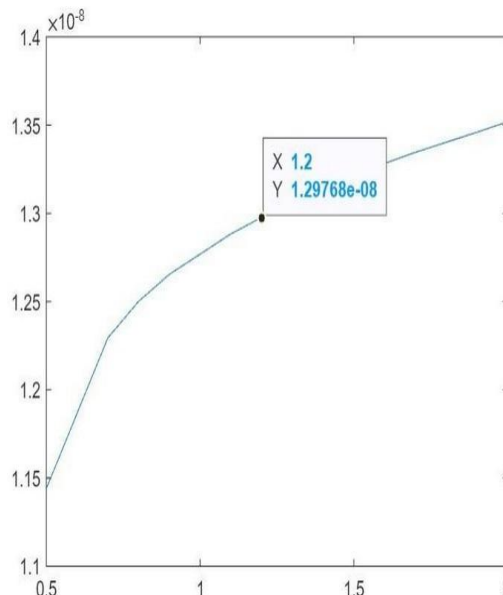
PROCEDURES:

- We must first identify the device structure that will be simulated (length, thickness, width of the channel, source and drain).
- We need to specify the properties of the material and provide the gate oxide, source and drain (doping concentration, relative dielectric constant, etc.)
- The option to fix parameters must then be chosen.
- For one or more models that you fit the data, parametric fitting entails identifying coefficients (parameters).
- According to the kinds of features that need to be mimicked, the biasing conditions need to be provided (Output or Transfer characteristics).
- The results may then be retrieved either as values or as a graph picture when we've completed our simulation.
- We may display those numbers and show the simulation outcome in Matlab.

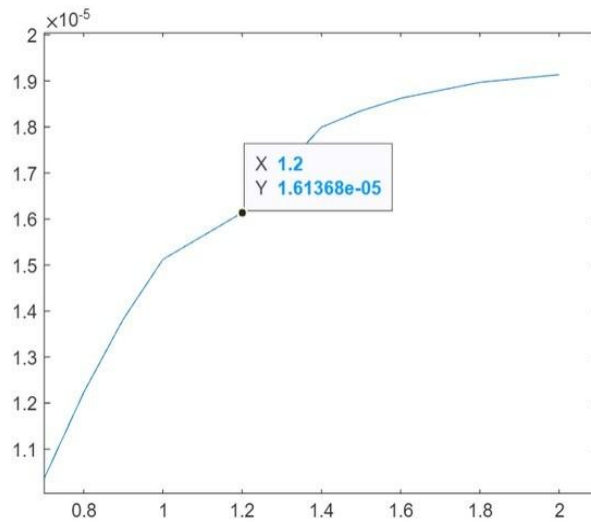
RESULTS

OUTPUT CHARACTERISTICS:

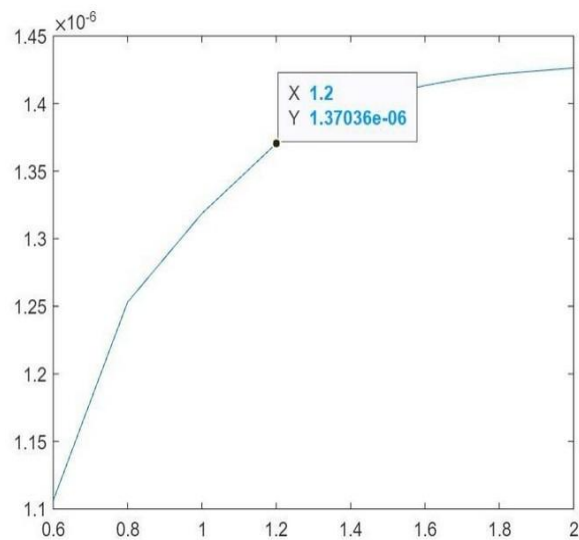
When I_D and V_{DS} vary, the value of V_{GS} also changes, and this is defined by the output characteristic. The drain current versus gate-source voltage is plotted in the transfer characteristic below.



At $V_{gs}=2V$,



At $V_{gs}=1v$,

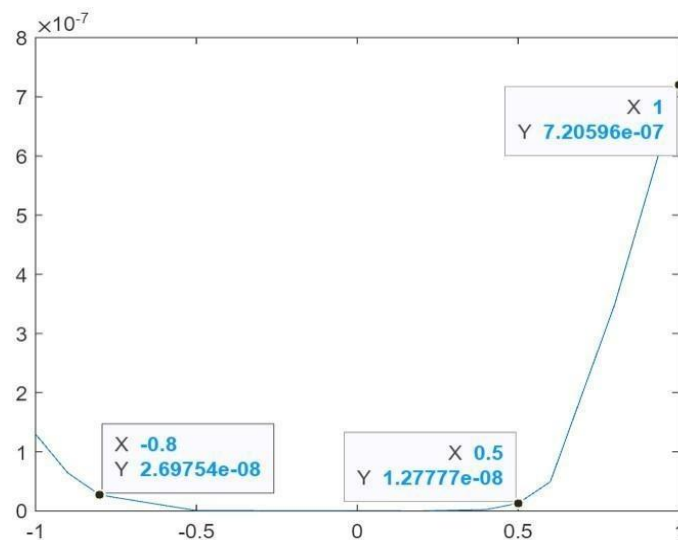


At $V_{gs} = 0.5 v$

TRANSFER CHARACTERISTICS.

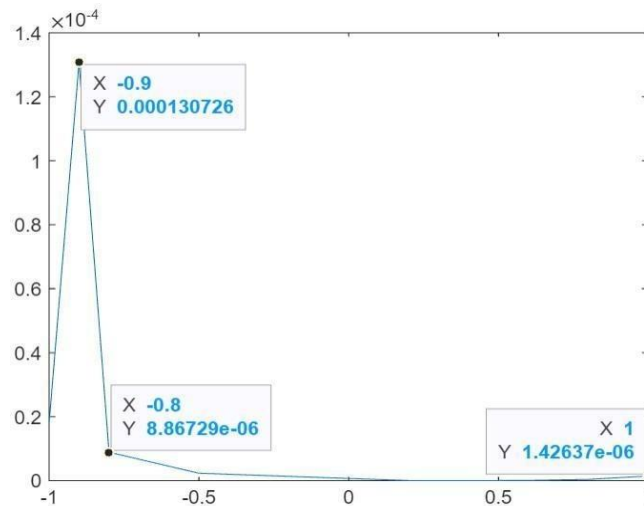
The change in the value of V_{DS} with changes in I_D and V_{GS} is defined by transfer characterist The transfer characteristic curve for drain current vs gate to source voltage is shown below.

At $V_{ds} = 0.5v$,



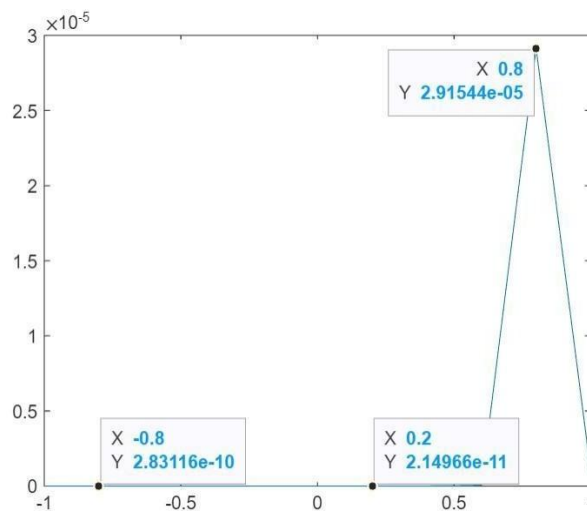
Vgs vs Ids when $V_{ds} = 0.5 V$

At $V_{ds}=1v$,



Vgs vs Ids when Vds = 1V

At Vds = 2v,



Vgs vs Ids when Vds = 2 V

5. CONCLUSION

Fin FET technology has taken nearly 20 years to develop and become a reality in the semiconductor industry, replacing planar devices. However, since technological progress does not allow for rapid changes, FinFETs benefit from advances in planar nodes, such as the high-K metal gate, elevated/epi source-drain, strained silicon, and gate-load process. It is widely believed that Si or SiGe FinFETs could be replaced by TFETs, although it is unclear whether technical advances will change significantly as they scale below 7-nmnodes.

Many organizations have explored the potential of TFETs using 2D materials, similar to conventional semiconductors. Initial results show that TMDC-based tunnel FETs have great potential due to their excellent gate control over the tunnel junction, scalability, broken-gap TFET architecture, and lack of TAT leakage; however, the technology still has a long way to go before it can meet the semiconductor industry's roadmap goals.

6. FUTURE IMPROVEMENTS

The future goal is to overcome Fin-based technologies by TFET to enable a smooth transition from FinFET technology to Fin-based vertical tunnel FETs while maintaining the advantages of FinFET design. To achieve this, a Fin Enable Area Scaled Tunnel FET, known as ASF-TFET, has been proposed. This device operates on the same principles as line TFETs, but has large gate control over the channel and tunnel junction, which greatly enhances performance. According to the simulation results, ASF-TFET provides 100% improvement in ON current, 15% reduction in OFF current, 3 improvement in transconductance, 30% increase in output resistance, 55% increase in unity gain frequency, and 6 reduction in footprint at a given drive capability for a gate length of 10nm.

Moreover, at 10 nm gate length, the proposed device lowers the average and lowest subthreshold swing (SS) to 40mV/dec and 11mV/dec, respectively. This paves the way for future FinFET system on chip (SoC) applications while improving analogue, digital and RF performance.

7. REFERENCES

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