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LOW-POWER RETENTIVE TRUE SINGLE-PHASE-CLOCKED FLIP-FLOP WITH REDUNDANT-PRECHARGE-FREE OPERATION

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ABSTRACT

As basic components, optimizing power consumption of flip-flops (FFs) can significantly reduce the power of digital systems. In this article, an energy-efficient retentive true-single-phase-clocked (TSPC) FF is proposed. With the employment of input-aware precharge scheme, the proposed TSPC FF precharges only when necessary. In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area. Post layout simulations based on SMIC 55-nm CMOS technology show that at a supply voltage of 1.2 V, the power consumption of the proposed FF is 84.37% lower than that of conventional transmission-gate flip-flop (TGFF) at 10% data activity. The reduction rate is increased to 98.53% as the data activity goes down to 0%. When the supply voltage decreases to 0.6 V, the proposed FF consumes only 0.411 fJ/cycle at 10% data activity, which is 84.23% lower than TGFF. Measurement results of ten test chips demonstrate the great energy efficiency of the proposed FF. Furthermore, the CK-to-Q delay of the proposed FF is 26.18% lower than that of TGFF at a supply voltage of 1.2 V.

1. INTROUCTION

With the development of the process, the performance of digital system is greatly improved, and the power consumption is becoming an important limitation of digital systems. In addition, with the rapid development of the Internet of Things (IoT), IoT devices are deployed on a large scale [1]. In such battery-powered or self-powered devices, low-power design becomes the focus of attention [2]–[5]. As basic components, the power of flip-flops (FFs) accounts for a large part of the power of digital systems [6], [7]. Therefore, reducing the power consumption of FFs can significantly reduce the power consumption of the digital systems.

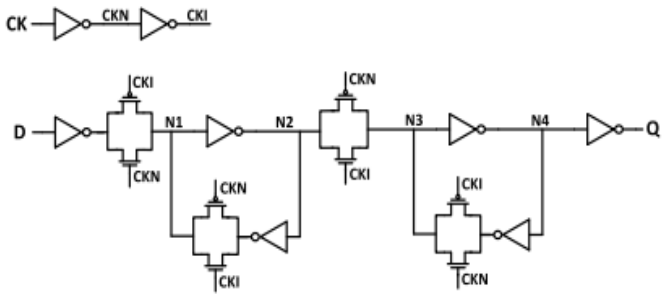

Fig. 1. Schematic of TGFF

Voltage-scaling technique has been proved to be an attractive method to decrease the power consumption of digital systems [8]–[12]. In order to obtain the power benefits of voltage-scaling technique, it is necessary to design an FF capable of operating at both super threshold and near/subthreshold supply voltage.

The transmission-gate flip-flop (TGFF) is the most widely used FF in current digital systems. The schematic of TGFF is shown in Fig. 1. The TGFF is a contention-free FF which is suitable for near-threshold operation. The main drawback of TGFF is the large clock network. The internal nodes CKN and CKI toggle no matter what the input data is, and the nodes CKN and CKI drive a larger number of transistors. Thus, the power consumption of TGFF is still large even if the data activity remains low. To reduce the power consumption of FF, the use of complementary clock signals should be optimized. Many low-power single-phase-clocked FFs have been proposed in previous works [13]–[18]. But there are still some problems that affect the power consumption of these FFs. For example, some of the FFs fail at low supply voltage [13]–[16], [18], and some suffer from large precharge power [13], [16]–[18]. In order to solve these problems, a lowpower true-single-phase-clocked (TSPC) FF is proposed in this article. The proposed FF is contention-free and suitable for wide supply voltage operation. Furthermore, redundant precharge operation is totally removed in the proposed FF and the power consumption is further optimized compared with previous low-power FFs

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2. OBJECTIVE

In this paper, an energy-efficient retentive True Single-Phase-Clocked (TSPC) FF is proposed. With the employment of input-aware pre charge scheme, the proposed ITSPC FF pre charge only when necessary. By adopting this technique, power consumption is minimized.

3. PROPOSED METHODOLOGY

In this Paper, an energy efficient retentive true single-phase-clocked (TSPC) FF is proposed. As basic components, optimizing power consumption of flip-flops (FFs) can significantly reduce the power of digital systems. With the employment of input-aware precharge scheme, the proposed TSPC FF precharges only when necessary.

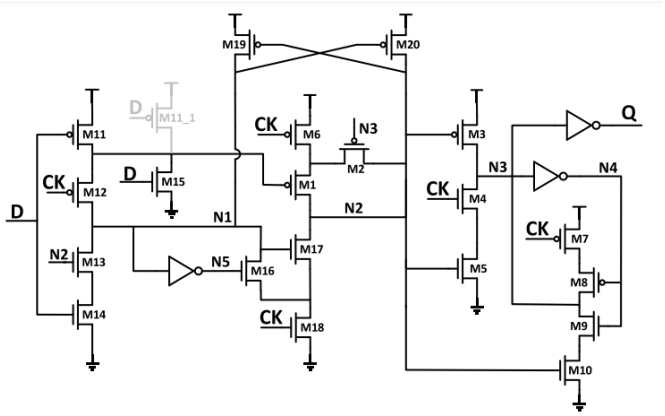

Fig 2: Schematic Design of the proposed TSPC FF

In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area. Later, the flip-flop is modified by adding SET, RESET scan inputs and finally a soft error tolerant Flip-flop is designed. The proposed designs are implemented in Tanner EDA/Cadence Virtuoso using 45mm technology file.

3.1 Design of Soft-Error Tolerant Optimization of the Proposed FF

Although scaling down the supply voltage can significantly decrease the power consumption of digital systems, aggressive voltage scaling will increase the soft error susceptibility of the systems [19]. In order to improve the stability of low-voltage systems, the proposed FF can be hardened to resist the single event effect (SEE), which includes single event upset (SEU) and single event transient (SET) [20]. The schematic of the proposed SEU-tolerant FF is shown figure below.

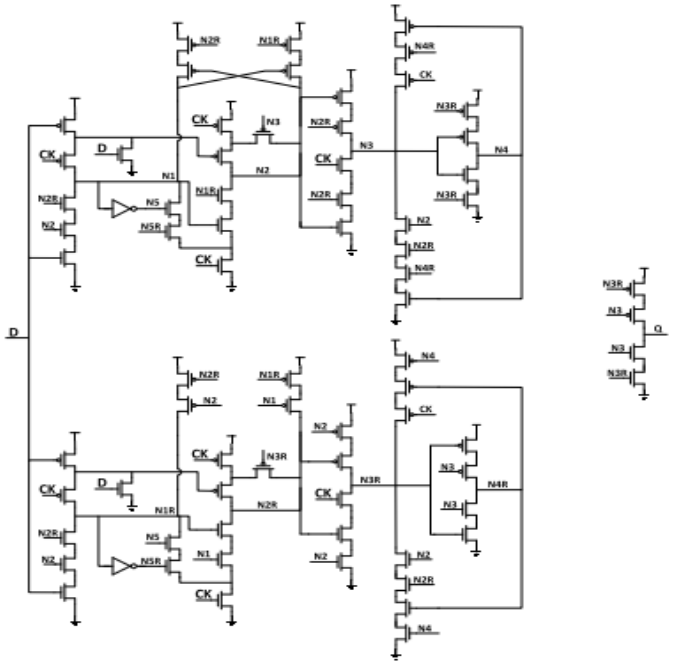

Fig 3: The schematic of the proposed SEU-tolerant FF is shown figure below

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This is because when the voltage of N2 drops from VDD to GND due to an SEU, M3 and M19 are ON, the nodes N3 and N1 are charged to VDD, and the data stored in the FF is overwritten. Similarly, the nodes N1, N3, N4, and N5 in the proposed FF are all susceptible to SEUs. C-element-based logic has been proved to be an effective method for hardening [21]–[23]. By using C-element based logic, the proposed FF can be insensitive to SEUs.

4. SIMULATION RESULTS

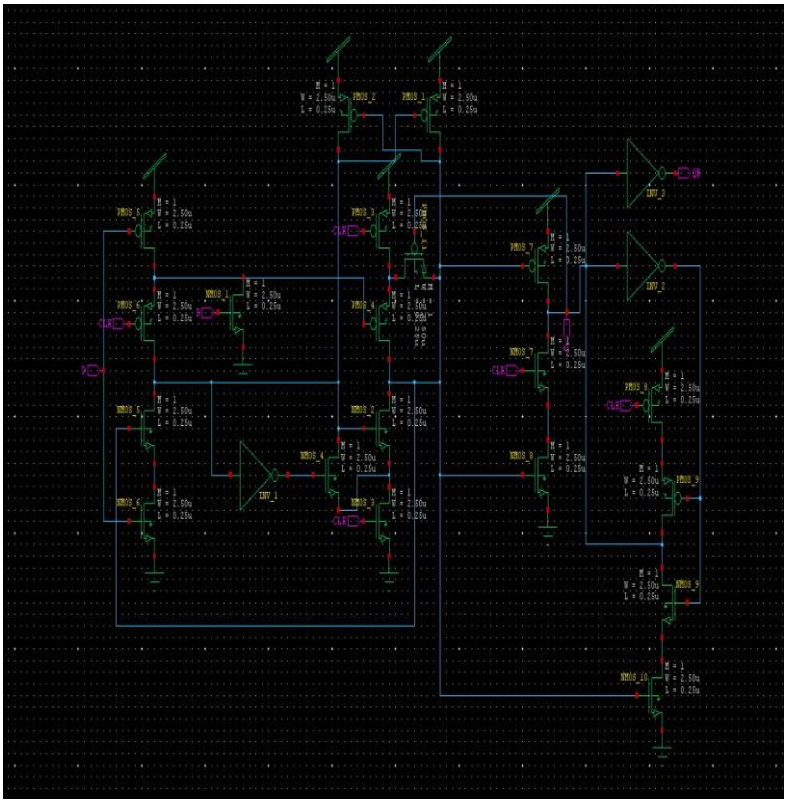

Fig 4: Schematic Diagram of True Single Phase Clocked FF (TSPCFF)

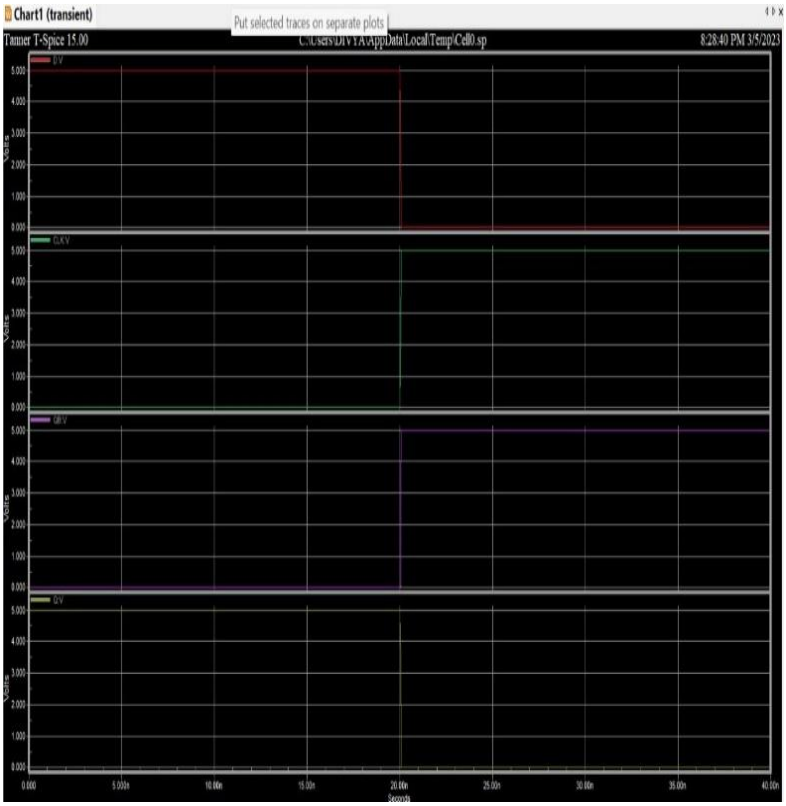

Fig 5: Output Waveform of True Single Phase Clocked FF (TSPCFF)

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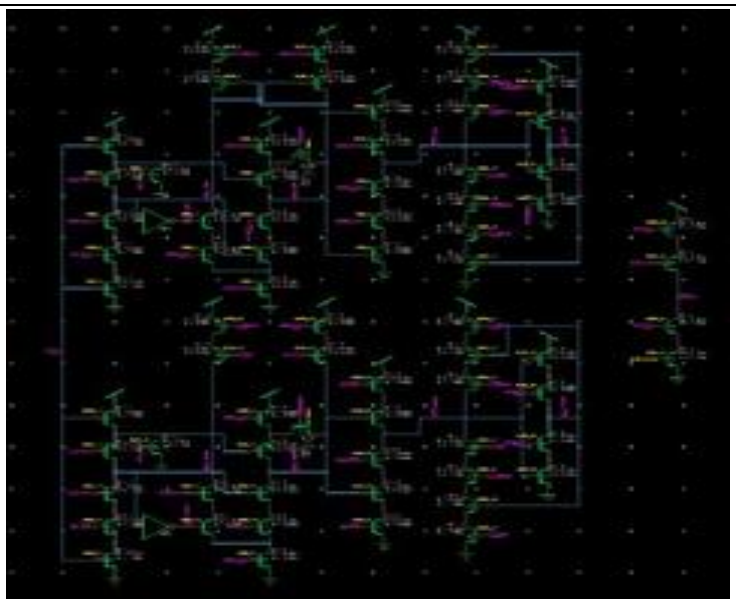

Fig 6: Schematic of the Proposed SEU-Tolerant FF (SEU-TFF)

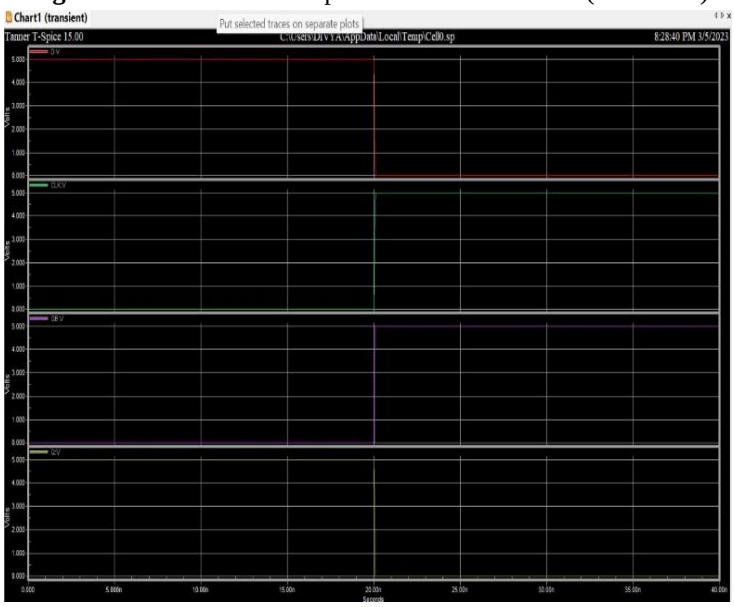

Fig 7: Output Waveform of Proposed SEU-Tolerant FF (SEU-TFF)

5. CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

An energy-efficient retentive TSPC FF was proposed. By removing redundant precharge and discharge operations with the input-aware precharge scheme, the power of the proposed FF is greatly reduced. Furthermore, floating node analysis is applied to the proposed structure to avoid the generation of short-circuit paths. Then, transistor level optimizations are applied to the circuit to further reduce the area and power consumption. Post layout simulation results show that the proposed FF saves more than 80% power consumption compared with TGFF under 10% data activity. Measurement results of ten test chips also demonstrate that the proposed FF has a significant energy efficiency improvement compared with TGFF. The CK-to-Q delay of the proposed FF is 26.18% lower than that of TGFF. The area of the proposed FF is just 4.8% larger than that of TGFF, indicating little area overhead to achieve such benefits.

5.2 FUTURE SCOPE

Further we would compare them and show that the counter designed with TSPC logic d flip-flop is less power consuming than other flip-flops. The circuit is then optimized at the transistor level to further reduce its size and power usage. According to post layout simulation results, the suggested FF consumes less power than TGFF with less than 10% data activity.

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