OPTIMIZING POWER EFFICIENCY IN ADDER CIRCUITTHROUGH GATE DIFFUSION INPUT TECHNIQUES AND THEIR APPLICATIONS

B. Sai Charan[1], Konkyana Lalitha Bhavani[2], Jayalakshmi Anem[3]

[1]M. Tech scholar at Department of E.C.E, Aditya Institute of Technology and Management, Tekkali, India

[2,3]Department of E.C.E, Aditya Institute of Technology and Management, Tekkali, India.

ABSTRACT

The world of today is all digital. The two biggest issues with digital gadgets are battery life and speed. There are several approaches of constructing the devices to get around these problems. One low power design method is Gate Diffusion Input (GDI). This study examines the most recent development in the field of low power designing, the GDI method. For this inquiry, a large number of publications are evaluated. Modeling, application, and the construction of the GDI cell are all reviewed. This report also verifies a comparison of the GDI approach with other designing techniques. Digital circuit designs are created using TANNER S-EDIT 12.0 tools, and simulation is performed with TANNER SPICE 15.0 version tool. When compared to other approaches such as PTL, GDI, and MGDI techniques, the power dissipation and power delay in CMOS design are significantly higher. By using the low power design methodologies of GDI and MGDI [6], transistor count and area will be decreased. Using the newest GDI methods is the aim of this article. This studyshows that the main use of this technology is in digital circuits.

Key words: Gate Diffusion Input, low power designing, alternative designing techniques

1. INTRODUCTION

The Full Adder Cell is a crucial component of Digital Signal Processors (DSPs), Application Specific ICs (ASICs), Digital Processors, and so on. Improving the performance of the 1-bit full adder has a positive effect on the system's overall performance. Therefore, the development of complete adders with low power consumption and excellent performance is crucial. Speed has been utilized as a performance measure by VLSI designers. Generally speaking, high performance area unit 2 and little space are competing restrictions. One of the two distinct reasons why the capacity used for a given performance in a CMOS circuit should be decreased is to reduce chilling, which willenable an excessively high function density to be integrated on an IC chip. As long as power dissipation doesn't negatively impact circuit performance overall, any amount of it is worthwhile. When average power is measured in microwatts, battery-operated instruments are equivalent to electronic watches. The square of the availability voltage in CMOS circuits is directly correlated withswitch activity, electrical phenomenon loading, and ability consumption. One of the most important components of any processor is the full adder, which is used in floating-point, the arithmetic logic unit (ALU), digital signal processing, image processing, video processing, microprocessors, and all arithmetic operations such as division, multiplication, and subtraction. Improving a 1-bit Full Adder[7] cell's performance can significantly boost the system's overall performance.

2. GATE DIFFUSION INPUT TECHNIQUE

Gate diffusion input is a design technique used in complementary metal-oxide-semiconductor (CMOS) circuits. It allows for the more power-efficient creation of logic gates by making the most of transistor utilization. Every logic gate in conventional CMOS logic—AND, OR, NAND, NOR, etc.—needs a certain configuration of PMOS (positive-channel MOS) and NMOS (negative-channel MOS) transistors. GDI makes this easier by taking a more adaptable tack. GDI uses a single type of gate structure that can be modified to execute different logic functions, as opposed to creating each gate from scratch.A modified CMOS gate structure is used by GDI [10]. It decreases the number of transistors required for some logic tasks by combining PMOS and NMOS transistors. The gate diffusion input approach in a typical GDI setup makes use of a unique transistor design in which the input signals control the gates of both the PMOS and NMOS transistors.Various logical operations can be produced by the GDI approach by applying the right input signals. This is accomplished by reducing the number of transistors and power consumption by sharing a single source or drain node.
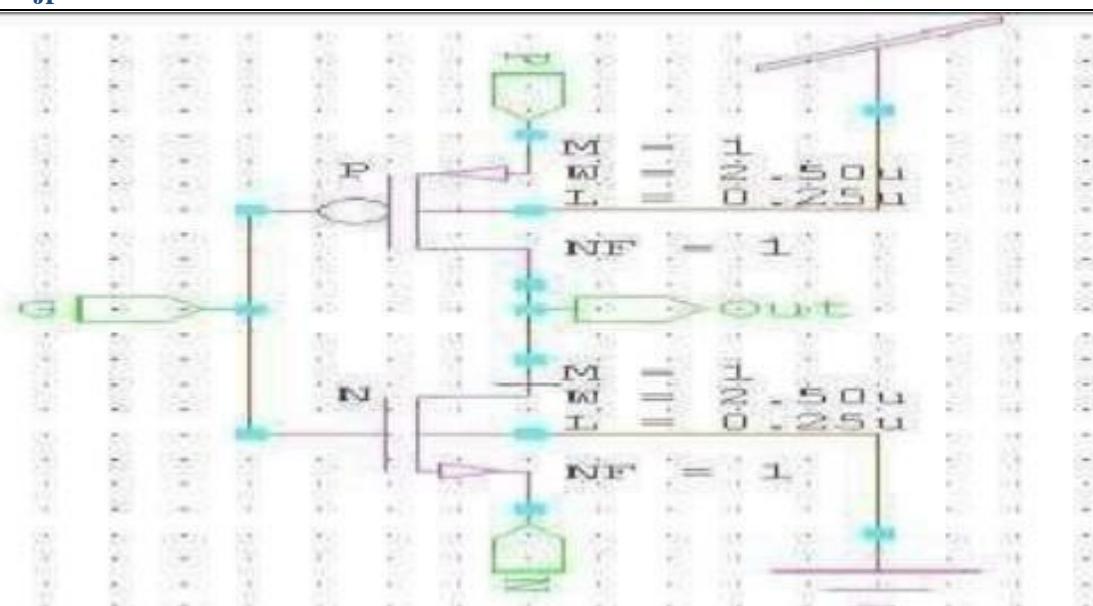
Fig.1 PMOS & NMOS design using GDI

The GDI approach is predicated on using a basic Although the fundamental cell initially looks similar to a typical CMOS inverter, there are a few key distinctions. 1) According to Figure 1, the GDI cell has three inputs: N (input to the source/drain of nMOS), P (input to the source/drain of pMOS), and G (common gate input of nMOS and pMOS). 2) Unlike a CMOS inverter, bulks of nMOS and pMOS are connected to N or P, respectively, meaning that they can be arbitrarily biased. The PTL methods now in use differ from the GDI cell structure. It should be noted that while some functions may be effectively implemented in twin-well CMOS or silicon, others cannot be performed in conventional p-well CMOS technologies.

3. MODIFIED GDI PRIMITIVE CELLS

The fundamental building block of a GDI cell is made up of two transistors, nMOS and pMOS, with four terminals: G, which is the common gate input of the two transistors; P, which is the pMOS transistor's outer diffusion node; N, which is the MOS transistor's outer diffusion node; and D, which is the common diffusion node of the two transistors. This study presents the implementation of modified primitive GDI logic gates in 0.250μm technology, along with a comparison with current GDI and CMOS logic. The functioning of the AND gate is explained with an example. For AND gate the drain of pMOS is -off and nMOS in linear pMOS in linear and nMOS in cut-off linear and nMOS in linear thereby producing the output as 1. The logical level for different input combinations will be: For A=0 and B=0: pMOS in Linear: Vin Vtp < Vout < VDD.
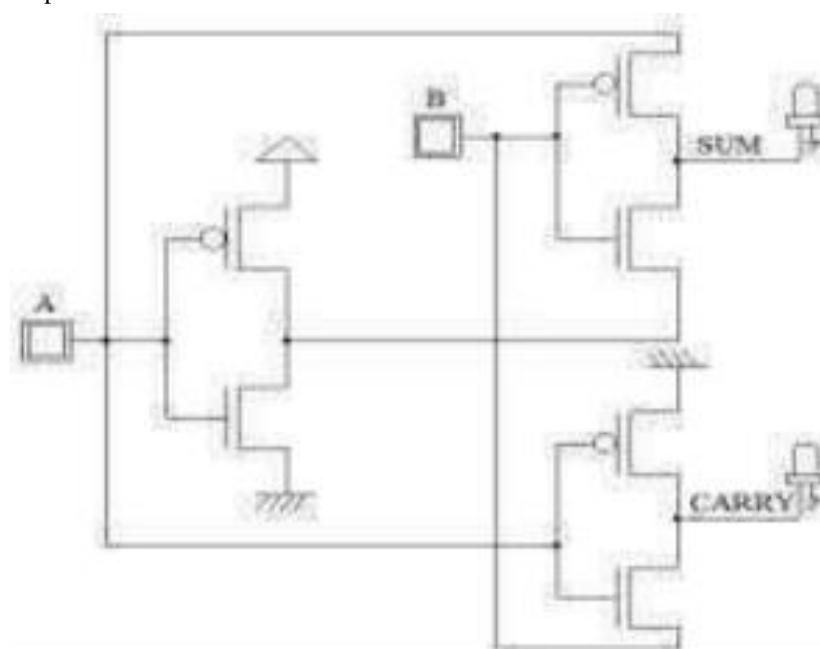
Fig.2 Half adder using GDI
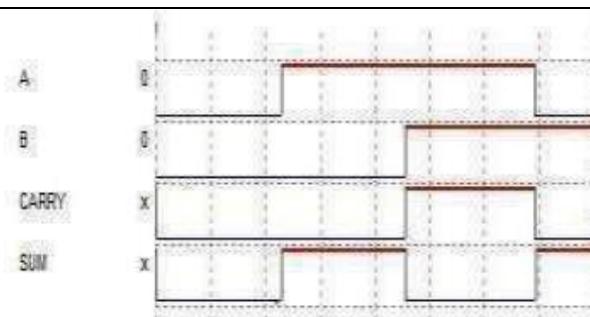
Fig.3 Half adder using GDI Waveforms

Using GDI techniques to construct the circuit to accomplish the half adder function is the first step in implementing a GDI (Gate Diffusion Input) cell for a half adder. A simple digital circuit known as a

half adder is used to calculate the total and carry-out of two binary values with one bit each. You will build XOR and AND functions using GDI gates in order to develop a half adder using GD

4. SIMULATION RESULTS

The designs are done in TANNER S-EDIT 12.0 tools and simulated using TANNER SPICE 15.0 version tool.
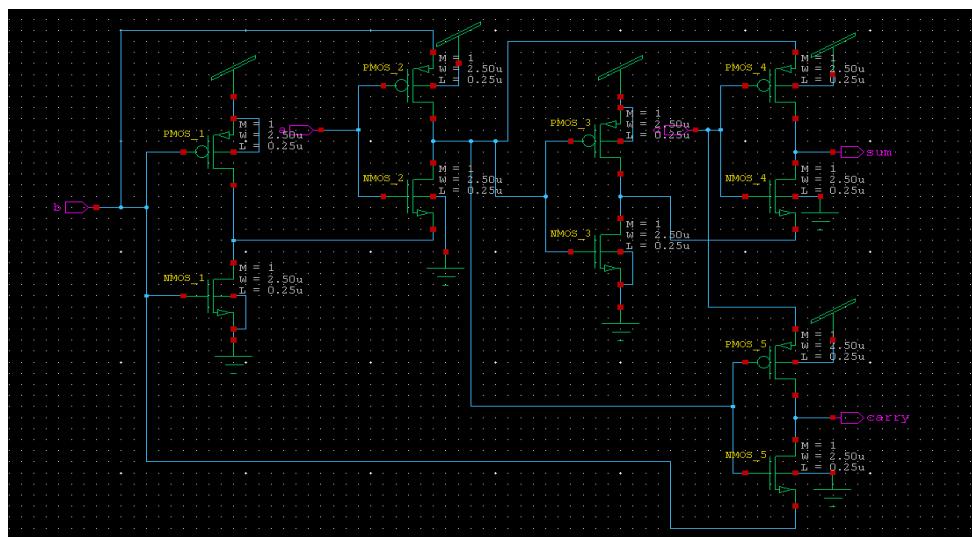
Fig:4. FULL ADDER using GDI

Fig.4-The GDI logic for the whole adder is shown in Fig. 4. Compared to CMOS, AND and OR gates have fewer transistors in their design. An N-MOS transistor and a P-MOS transistor are used in a certain arrangement to create a basic AND gate setup. In GDI logic, an OR gate can be built with less transistors by employing a particular layout. A Full Adder implemented with GDI logic is shown in Fig. 5; it makes use of the effectiveness of GDI gates to create a small and power-efficient architecture. by carefully utilizing GDI approaches to create AND, OR, and XOR gates.
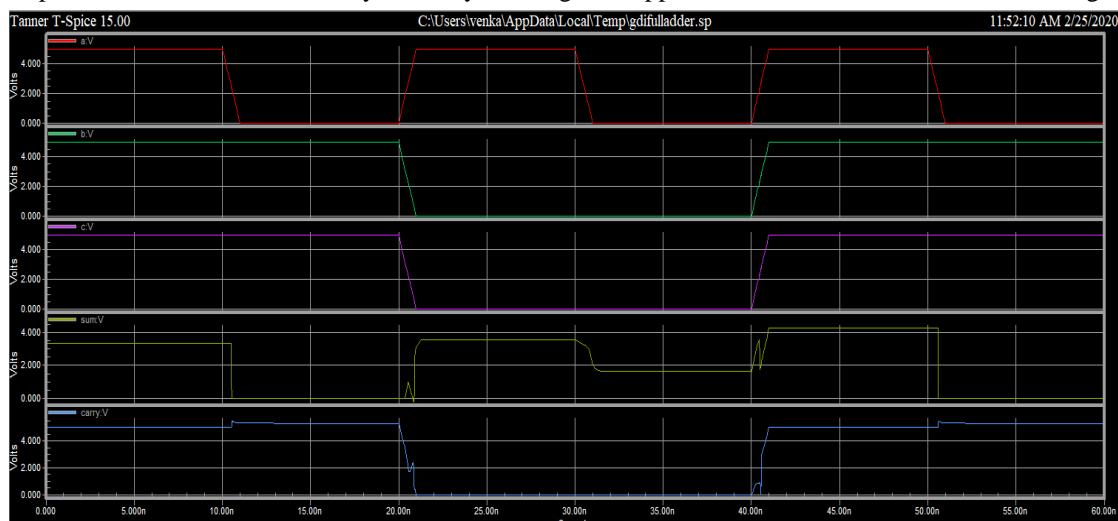

Fig: 5 FULL ADDER output using GDI

5. COMPARATIVE RESULTS OF VARIOUS TECHNOLOGIES :

The TANNER SPICE 15.0 version tool is used to simulate the designs, which are completed in TANNER S-EDIT 12.0 tools. Digital gadgets require fast speeds and low power [3] usage. When compared to other approaches such as PTL, GDI, and MGDI techniques, the power dissipation and power delay in CMOS design are significantly higher. By using the low power design methodologies of GDI and MGDI, transistor count and area will be decreased. When compared to CMOS, the GDI design dissipated less power.Table 1 illustrates how different logic gates and a full adder can reduce power dissipation by using GDI and MGDI. Table 2 displays the enhanced delay performance for different logic gates and full adders when employing GDI and MGDI.

Table-1

LOGIC GATES	CMOS (mW)	PTL(mW)	GDI(mW)	MGDI (mW)
AND	1.92	1.12	0.86	0.43
OR	7.83	1.62	1.22	1.12
XOR	8.44	4.05	3.65	3.32
MUX	6.75	4.37	2.09	1.82
FULL ADDER	10.62	6.24	4.31	3.79

Table -2

LOGIC GATES	CMOS(nW)	PTL (nW)	GDI (nW)	MGDI (nW)
AND	15.12	12.42	10.04	4.99
OR	19.94	15.13	10.07	5.11
XOR	9.96	9.77	5.10	4.85
MUX	14.92	10.24	9.98	5.80
FULL ADDER	19.01	9.95	7.52	4.90

6. CONCLUSION &FUTURE SCOPE

New methods for designing digital systems are constantly being developed as technology develops to meet the increasing demands for performance and efficiency. When compared to conventional CMOS designs, the Gate Diffusion Input (GDI) approach has been acknowledged for its benefits in terms of lower power consumption and transistor count. GDI is especially well-suited for low-power applications because to its efficiency, despite some issues like threshold leakage.

Future performanceand efficiency gains are anticipated thanks to the incorporation of GDI and MGDI approaches into digital circuit design. Further automating design processes aided by Gate Diffusion Input (GDI) cells and investigating technological compatibility with twin-well CMOS techniques can also lead to even more scalable and optimal solutions. In order to improve digital circuit design and satisfy thechanging needs of contemporary technology, future research and development should concentrate on utilizing these developments.

Gate Diffusion Input (GDI) and Modified Gate Diffusion Input (MGDI)approaches have a bright and diverse future ahead of them. As technology advances, these methods' performance and energy efficiency may be further improved by tailoring them for new domains like quantum computing and nano electronics.

The design process can be streamlined and development time decreased by creating standard cell libraries and advanced design tools that are optimized for GDI and MGDI. Improving circuit reliability requires finding novel materials and techniques to address threshold leakage.

Furthermore, these methods can be optimized by combining them with cutting-edge CMOS processes, such as twin-well CMOS. Compactness and power efficiency will increase in IJternet of Things (IoT) and wearable technology when GDI and MGDI [6] are used. Finally, integrating these methods into industrial training programs and academic curriculum will provide upcoming engineers with the skills necessary for innovative digital design.

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