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PERFORMANCE ANALYSIS OF TERNARY RIPPLE CARRY ADDER DESIGNS USING PROPOSED TERNARY 3:1 MUX AND PROPOSED TERNARY HALF ADDER

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ABSTRACT

This paper presents an innovative circuit design for a Ternary Ripple Carry Adder (TRCA) utilizing a newly proposed Ternary 3:1 multiplexer (3:1 TMUX) and a proposed Ternary Half Adder (THA) and Ternary Full Adder (TFA). This study aims to attain minimal power consumption and propagation latency in the proposed circuits. The suggested Ternary Ripple Carry Adder circuit is evaluated against existing circuits and exhibits enhanced performance according to their performance parameters. Circuit analysis and simulations were performed with the Tanner EDA design environment at a 90 nm technology node. The simulation findings demonstrate that the suggested designs surpass other existing circuits regarding latency and power-delay product (PDP), making them appropriate for high-performance ternary computational circuits.

Keywords- Ternary Logic, Ternary Ripple Carry Adder, Ternary 3:1 Multiplexer, Ternary Half Adder, Ternary Full Adder.

1. INTRODUCTION

Application-specific processing is advantageous compared to general-purpose processing due to the increasing demand for battery-operated advanced portable embedded electronic devices. The primary impediment to attaining the specified objective is rapid processing coupled with minimal power consumption. Presently, binary digital processing is employed, while multivalued logic systems may serve as alternatives to binary logic. The binary system, with a radix of 2, only employs the symbols 0 and 1. In multi-valued logic, the radix number can exceed 2, as exemplified by ternary logic, which employs a radix of '3' in its numerical system. The ternary number system employs the symbols 0, 1, and 2 to represent three logical states. Ternary logic is superior to binary logic for area optimization and speed [1]. Ternary logic can address speed and space challenges, as it enables a greater number of functional realizations with a given number of inputs compared to binary logic. Voltage levels effectively reflect ternary logic. The states 0, 1, and 2 correspond to voltage levels of 0, Vdd/2, and Vdd, respectively [2]. The subsequent advantages of ternary (base 3) reasoning compared to binary (base 2) logic are outlined.

2. THEORETICAL BACKGROUND

2.1 Ternary Logic Fundamentals

P and N-channel transistors complementary structures were employed symmetrically to provide three separate logic levels in the initial MOSFETs-based ternary (radix 2) basic gates design. The supply of power was significantly greater than the transistor's threshold voltage at the same time, which increased the intricacy of the circuit and the amount of power used [4-5]. The above-mentioned ternary circuits, which require the use of resistors, can result in a certain level of static power consumption. Due to this, situations have suggested two ternary basic logic gate design methods that use only four different types of MOS transistors and do not require resistors, hence lowering the circuit's static power consumption and simplifying the circuit's component list. At the same time, it shortens the propagation latency. One significant aspect is that ternary digital logic offers a new and practical approach to various applied difficulties. For instance, in the context of digital control circuits, ternary logic can be used to represent the "on," "off," and "idle" states of an item of equipment. Ternary logic consists of two categories: unbalanced representation techniques and balanced representation techniques [6]. The unbalanced ternaries include positive and negative ternaries with the logical sign-relevant numbers 0, 1, and 2. A balanced ternary is represented by the numbers 1, 0, and 1. In this tutorial, we'll focus on designing unbalanced ternary logic circuits [7-8].

2.2 The CMOS Ternary Gates

In ternary logic, three different types of inverter gates are possible: the STI (Simple Ternary Inverter) is standard inverter which is invert 'O' and '2' and 'l' is remain same, PTI (Positive Ternary Inverter) is only invert '2' and for remains give logic '2', and NTI (Negative ternary inverter) is only invert logic 'O' for remains it give logic '0'. Truth table of ternary

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inverter shown in Table 1. One input (x) and three outputs (ZO, Z1, and Z2), which stand for negative, standard, and positive ternary inverter procedures, make up the basic ternary gate (NTI, STI and PTI). These inverters equations are written out in Equation.

$$Z0 = \begin{cases} 2, & \text{if } Z = 0 \\ 0, & \text{if } Z \neq 0 \end{cases} \quad \text{---------- (1)}$$

$$Z1 = \bar{x} = 2 - x \quad \text{---------- (2)}$$

$$Z2 = \begin{cases} 0, & \text{if } Z = 2 \\ 2, & \text{if } Z \neq 2 \end{cases} \quad \text{---------- (3)}$$

Table 1: Truth Table of Ternary Inverter

Input	STI Logic Level	NTI Logic Level	PTI Logic Level
0	2	2	2
1	1	0	2
2	0	0	0

2.3 Logic Gates based on Ternary

T-NAND, T-NOR, and other ternary logics are also employed in a variety of circuits. Equations are provided below for certain logics.

$$P(AND) = Qi.Qj = \min\{Qi, Qj\} \quad \text{---------- (4)}$$

$$P(NAND) = \min\{Qi, Qj\}' \quad \text{----------(5)}$$

$$P(OR) = Qi + Qj = \max\{Qi, Qj\} \quad \text{----------(6)}$$

$$P(NOR) = \max\{Qi, Qj\}' \quad \text{----------(7)}$$

Table 2: Truth Table of the Ternary 2 input TNAND, TAND and TOR logic gates

A	B	TNAND	TAND	TOR
0	0	2	0	0
0	1	2	0	1
0	2	2	0	2
1	0	2	0	1
1	1	1	1	1
1	2	1	1	2
2	0	2	0	2
2	1	1	1	2
2	2	0	2	2

2.4 Combinational circuits based on Ternary Logic

If talk about binary half adder two radix number 0 and 1, if want to design 2 bit half adder can only represent 4outcomes. In ternary use 9 outcomes instead of 4 [1] [18]. If increase the bit value, the difference between binary and ternary is become large. Truth table of THA is given below in Table.

Table 3: Truth Table of Ternary Half Adder

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1

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2	2	1	1

1 to 3 Ternary decoder is one of the important building block in this work. This is crucial component since it can decode various input voltages and show that by making one of its output high ('2'). It features three output pins, numbered Out1, Out2, Out3, and a single input pin I. This decoder operates according to the logic shown in table 4.

Table 4: Truth Table of Ternary 1 to 3 Ternary Decoder

I	Out1	Out2	Out3
0	2	0	0
1	0	2	0
2	0	0	2

A Multiplexer is a circuit that, in response to a select control signal, choose one of its many inputs and transfer it to the output. Three inputs make up the Ternary 3 to 1 Multiplexer. I0, I1 and I2 using selection line S, anyone of the input can be sent to the output. Truth table of Ternary 3 to 1 Mux depicted in table 5.

Table 5: Truth Table of Ternary 3 to 1 Multiplexer

Selection Line	Outputs
0	I0
1	I1
2	I2

A 1 to 3 decoder is used to construct a ternary 3 to 1 mux. The decoder's input signals serves as the selection line for a 3 to 1 Ternary multiplexer.

3. PROPOSED WORK

3.1 Proposed Ternary Half Adder (THA)

The figure 1 depicts the Ternary Half Adder's diagram. Two DPL based TAND gates, a DPL based TOR gate, a 3:1 multiplexer, and a 3:1 decoder are used to build the Sum part of THA. The selection line S of the 3:1 TMUX receives one of the inputs of THA. Thus the input of the 1 to 3 decoder is affected by the other input B of the THA. First output "outl" of the decoder is the input to one of the and gates, and "A" is the input to the other. The output "out3" of the decoder serves as the input to the remaining TAND gate, and the other input is a constant logic "1". the initial 3:1 input.

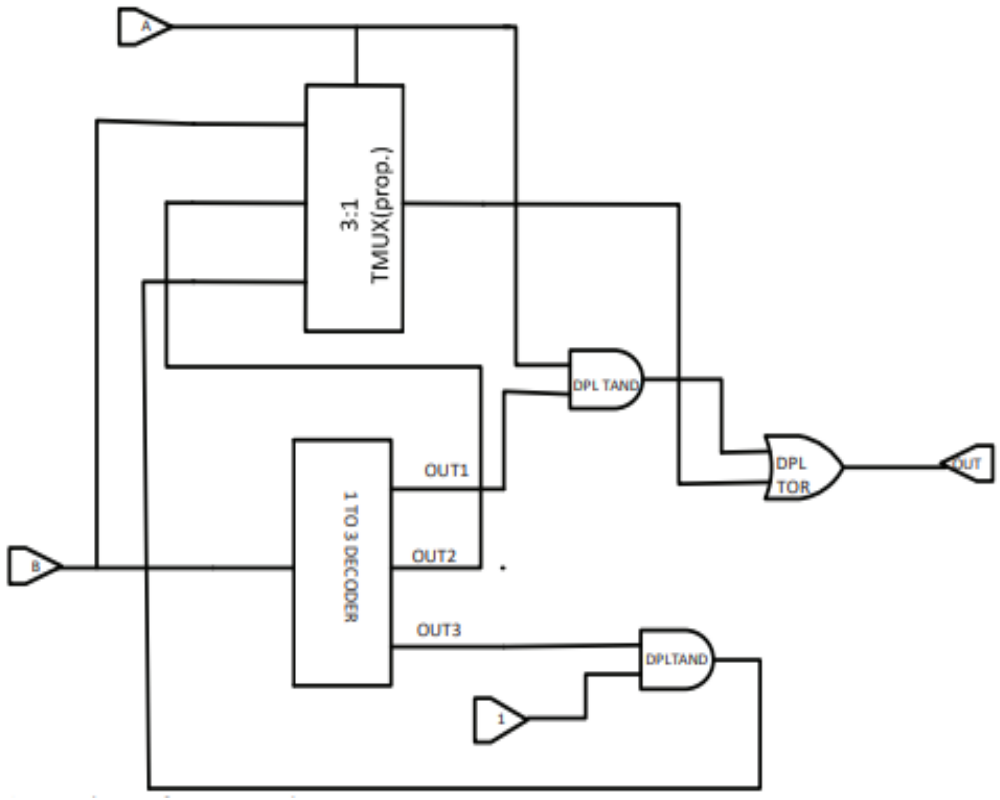

Figure 1: Design of proposed Ternary Half Adder

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3.2 Proposed Ternary Full Adder (TFA)

The figure 2 depicts the Ternary Full Adder's diagram. Two THA and TOR gates are used to design Ternary Full Adder. TOR is used to generate the carry and two THAs are used to generate the Sum.

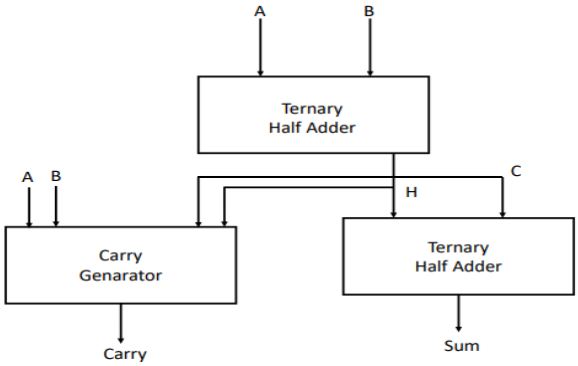

Figure 2: Design of proposed Ternary Full Adder

3.2 Proposed Ternary Ripple Carry Adder (TRCA)

The figure 3 depicts the 4-Bit Ternary Ripple Carry Adder's diagram. One THA and Three TFAs are used to design Ternary Ripple Carry Adder.

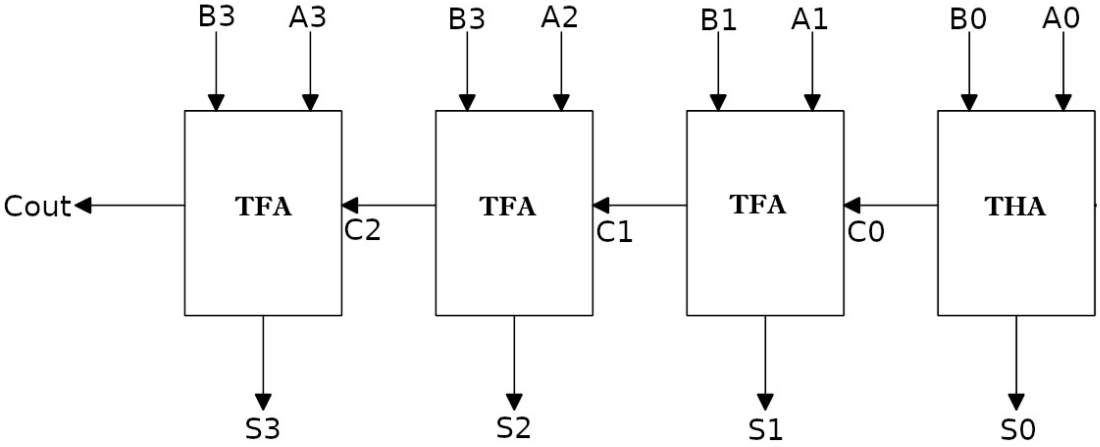

Figure 3: Design of proposed 4-Bit Ternary Ripple Carry Adder

4. SIMULATION RESULTS

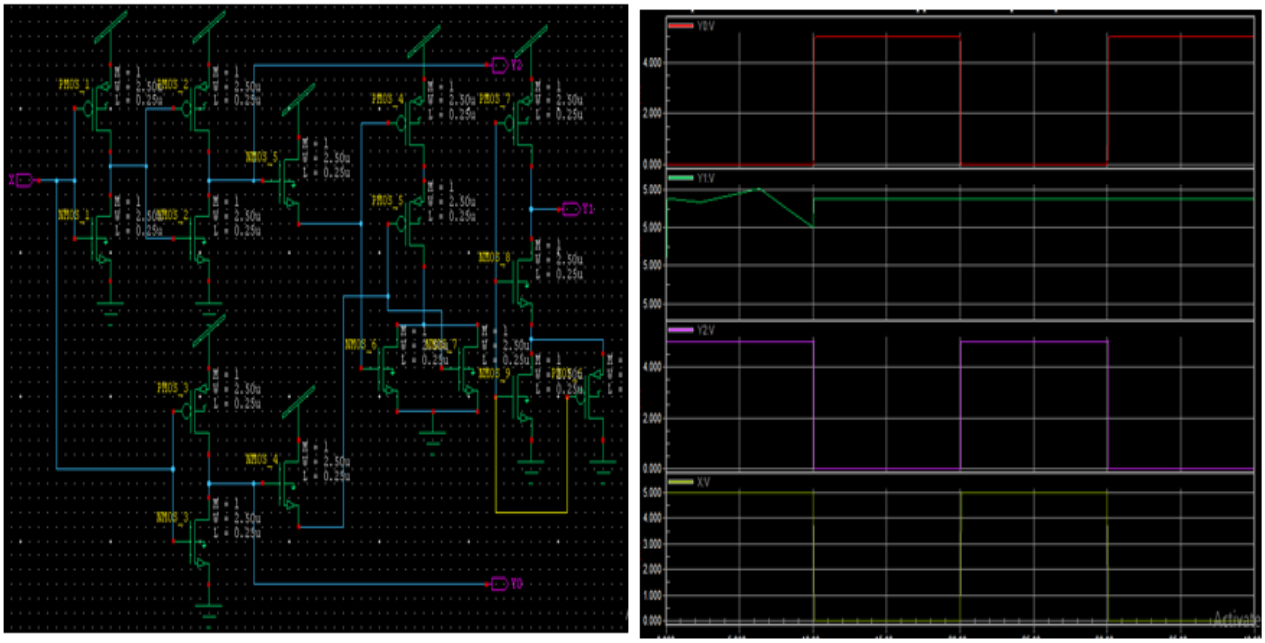

Figure 4: Proposed 1:3 Decoder Schematic diagram and output waveform

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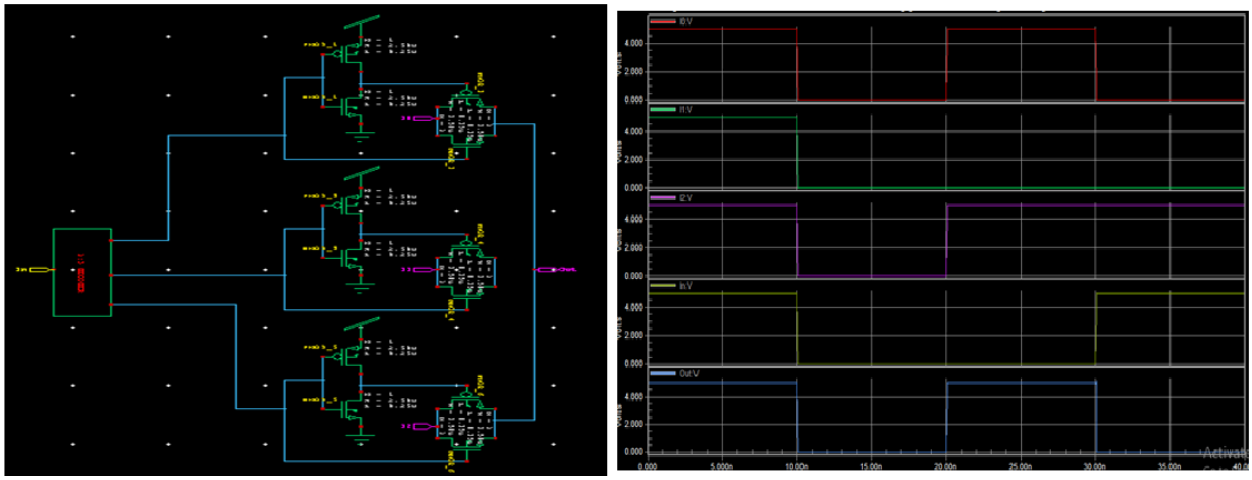

Figure 4: Proposed 3:1 Multiplexer Schematic diagram and output waveform

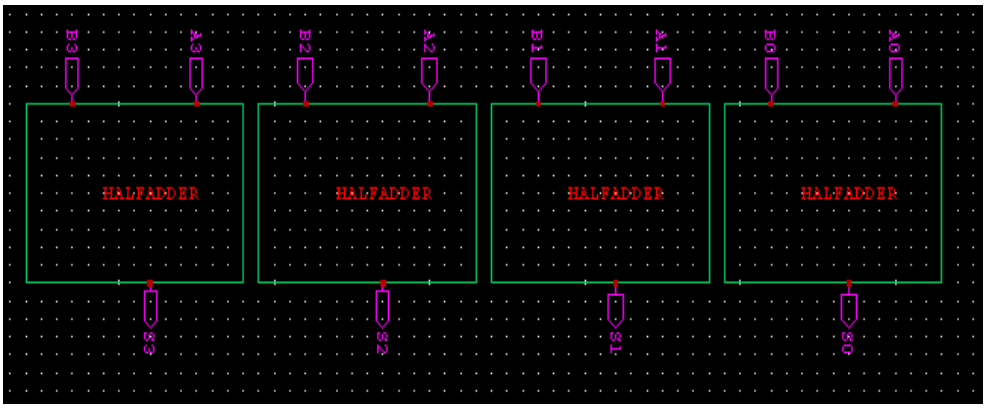

Figure 4: Proposed 4-Bit Ternary Ripple Carry Adder Schematic diagram

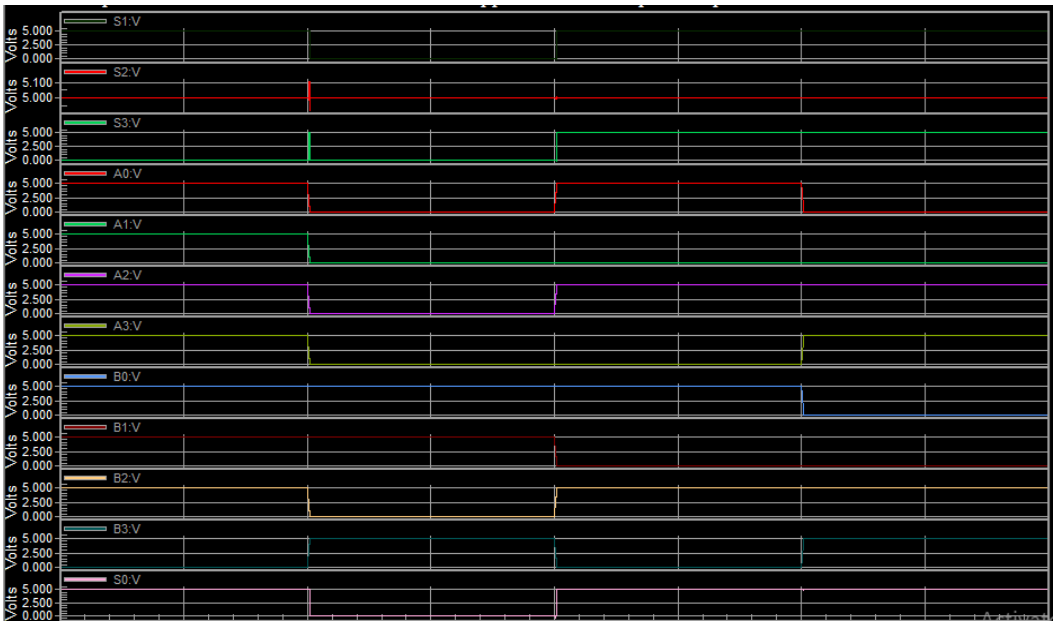

Figure 5: Proposed 4-Bit Ternary Ripple Carry Adder output waveforms

5. CONCLUSION

The innovative circuit for 4 Bit Ternary Ripple Carry Adder (TRCA) designed by using proposed Ternary Half Adder (THA) and Ternary Full Adder (TFA). The proposed circuits provide better result's compared the existing techniques like DPL and CMOS Logic. The suggested Ternary Ripple Carry Adder circuit is evaluated against existing circuits and exhibits enhanced performance according to their performance parameters. Circuit analysis and simulations were performed with the Tanner EDA design environment at a 90 nm technology node. The simulation findings demonstrate that the suggested designs surpass other existing circuits regarding latency and power-delay product (PDP), making them appropriate for high-performance ternary computational circuits.

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