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TRANSFORMERLESS THREE PHASE HIGH QUALITY MULTILEVEL INVERTER USING A COMMON DC SOURCE

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ABSTRACT

This research proposes a transformerless high-resolution hybrid asymmetrical multilevel inverter. A mix of the Level Doubling Network (LDN), cascaded H-bridge (CHB), and neutral point clamped (NPC) multilevel inverter (MLI) is the proposed topology. The proposed research intends to lower the inter array leakage current and dc-bus capacitor demand by merging all three of the main bridge's dc buses using TNPC. The primary difficulty with this hybrid transformerless converter architecture is matching the correct LDN operation to the TNPC capacitors. One more low-rated non-isolated buck-boost converter and a closed-loop current control are utilized for the capacitor balancing of TNPC, which will ultimately assist in getting rid of a large, pricey transformer. With an extra converter that only has a rating of 7% to 8% of the transformer rating, it will assist to save both capital and operating costs. Compared to other asymmetrical MLI topologies with identical resolution at output voltage, this architecture provides higher power quality, reliability and efficiency with fewer components. Utilizing the MATLAB/Simulink model, simulation was carried out and outcomes closely resembled concept.

Key words: Photovoltaic (PV), asymmetrical multilevel converter, level doubling network (LDN), capacitor balancing, open loop control and multilevel converter (MLI).

1. INTRODUCTION

In order to fulfill energy needs, multilevel inverters are becoming more and more common in medium voltage, high power applications [1]. The creation of innovative inverter topologies to boost power quality and increase device usage is the main focus of right now. In two level [2] or three level inverters [3], high switching frequencies are required to ensure power quality. Alternatively, bigger filters can be used, although this approach adds to the systems complexity and expense. High resolution multilevel inverters [4]– [5] can address problems with filter losses, efficiency, dependability and power quality. The terms flying capacitor (FC), diode clamped (DC), and cascaded H bridge (CHB) multilevel inverter refer to three fundamental multilevel inverter topologies. Capacitor balance, uneven voltage stress on switches, a greater number of switches and DC sources, among other problems, are the primary causes of these topologies. CHB is the most often used multi-level inverter topology because of its scalability and versatility. A larger number of bidirectional DC sources were needed for the symmetric cascaded H bridge multilevel inverter.

Transformers are an essential part of the connection between the inverter and the grid in grid-connected solar PV applications. It aids in reducing leakage current and improving output voltage. However, because of the large and heavy transformer, the systems efficiency decreases and its weight, size, cost and complexity all rise. Thus, a great deal of research has been conducted to improve efficiency and create transformer-less inverter topologies [6].

Leakage current is effectively reduced using neutral point clamped inverters [7]. The midpoint of the NPCMLI DC-link capacitors is connected to the grid neutral to prevent common mode voltage. The active NPC (ANPC) multilevel inverter architecture in [8] is achieved by substituting switches for diodes. In comparison to a traditional NPC, it aids in sharing the stress and losses in switches equitably. Better performance, such as easy operation, reduced switching losses and overall volume reduction are demonstrated by TNPC [9] in comparison to NPC and ANPC. On the other hand, the outer leg of the three level-TNPC exhibits significant conduction losses. To eliminate filters between the inverter and transformer, a 5-level T type neutral point clamped inverter is presented in [10]. Transformer avoidance is not possible in this setup and a large number of switches are needed to provide adequate power quality.

Higher levels are provided by asymmetrical converter topologies [11] than by symmetrical ones. However, because of the uneven power distribution, it also presents difficulties and calls for a greater number of dc sources. With fewer switches, the topology proposed in [12] can produce output with 17 voltage levels. But it will put a lot of strain on the

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switches, and it also needs many dc sources. The literature discusses a number of hybrid topologies [13]– [14] for PV-fed grid-connected systems in an effort to increase power quality and efficiency. In order to attain high resolution and lower costs and losses, a mix of NPC and CHB is used in [13].

In the research, a double LDN-based architecture for grid-connected central inverter applications is presented [15]. The three DC busses in [15] are combined using isolation transformers, which reduces the size of the capacitor and the number of cables. Fortunately, this topology necessitates more sources, raising the systems cost. Because of this, auxiliary sources are eliminated in [16] at the expense of a few levels.

In these dual LDN-based topologies, the isolation transformer is required to join the major bridges. To increase system efficiency and lower system costs, these isolation transformers are eliminated in this study. The three phase TNPC is used to replace the three phase H bridges in the topology [15]– [16] in order to accomplish that. Level doubling network operation presents a significant issue with this hybrid topology: TNPC capacitor balancing. To balance the capacitor voltages, one more converter with closed loop control is suggested in this work. It is discovered that this supplementary converter can handle power at a rate of around 7% of the primary converter. Therefore, the three isolation power transformers can be replaced by a smaller, non-isolated dc-dc converter whose cumulative power rating is equivalent to the main converters rating.

Previous Art

The research proposes LDN, which produces a five-level output voltage by adding one half bridge to one full bridge. The floating capacitors that feed these half bridges are self-balancing, as seen in Fig. 1(a).

When working with a small number of switches, many LDN-based topologies can yield excellent resolution. But it has been discovered in earlier research that there are some limitations to various LDN-based topologies that employ a complete bridge in the primary DC bus: For all three major bridges to be fed by a single source, an isolation transformer is needed in each phase. The use of a transformer to combine the dc buses of three distinct phases has been discovered in the literature [15] to lower inter array leakage current, ripple current and the need for a capacitor. Fig. 1(b) displays the circuit diagram for combining the three phases dc buses with the isolation transformer. A significantly greater number of cable sets must be pulled from the field in order to have separate DC buses for each of the three phases. In partial shade conditions, it results in an imbalanced current injection into the grid and increased installation costs. Therefore, combining the three DC buses is a wise move. It is impossible to combine LDN-based topologies without electrical separation.

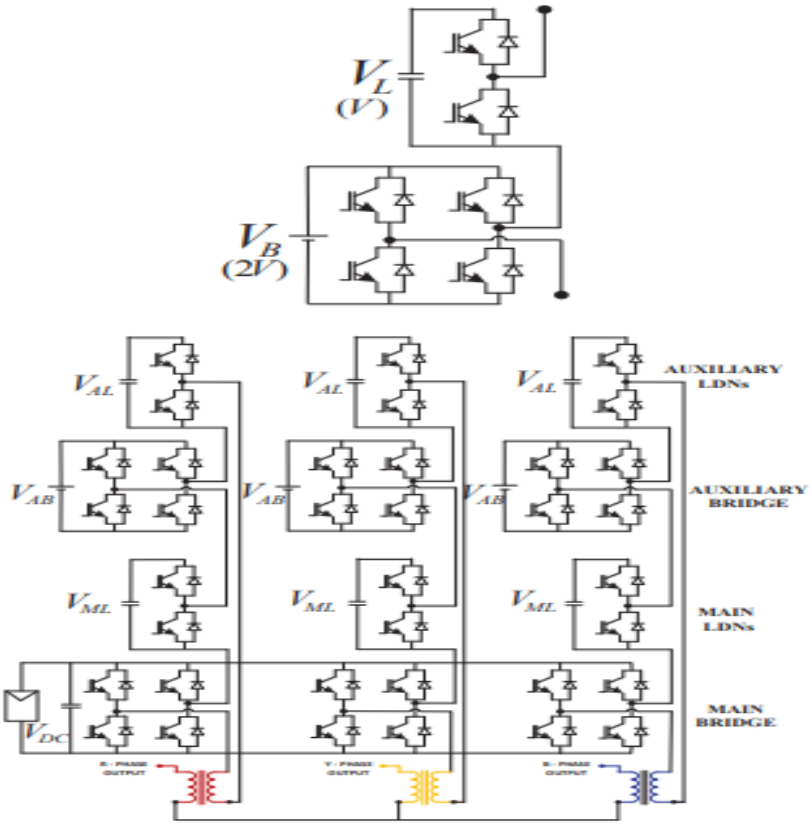

Fig. 1. (a) Single-phase module circuit schematic and (b) three-phase module circuit diagram in [15]

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The intention of combining and eliminating the transformer in three stages is to reduce the number of cables needed for PV arrays and other applications where isolation is not cost-effective to just one set. Transformers are required in some applications, while they are not required in others for the purpose of isolation. Such topologies allow for the removal of transformers. It is discovered that merging the three DC buses is feasible if the complete bridges of the main DC bus are replaced with NPC. TNPC is the most economical and efficient of all NPC-based topologies. Therefore, in this article, high voltage H bridges are replaced by TNPC.

Capacitor Balancing and Converter Structure

High resolution with fewer components is possible with the double LDN based architecture. An isolation transformer is used to combine the primary bridges of these topologies. To get a cost-effective converter solution, the primary goal of the suggested hybrid converter topology is to eliminate these isolation transformers. The isolation transformer is removed by replacing the topologies primary bridges with a three-phase TNPC, as seen in Figure 2. In the whole design, only one DC source will be needed when the DC buses of the major bridges are combined. The suggested hybrid topology's single and three phase modules are shown in Figs. 2(a) and (b), respectively.

The proposed converter topology uses the 1:5 ratio of asymmetry, which is the best ratio for the whole range of modulation indices. 43 levels at a unity modulation index can be attained with this ratio of asymmetry. The primary module in Fig. 2(b) consists of the main bridge and the main LDN, whereas the auxiliary module consists of the auxiliary bridge and the auxiliary module.

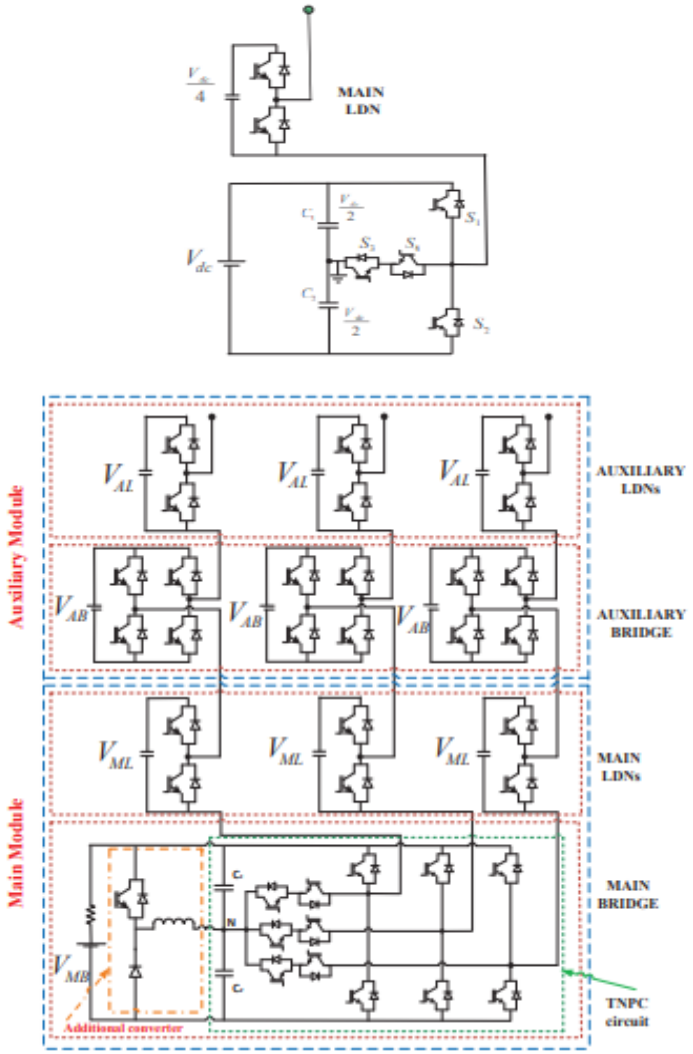


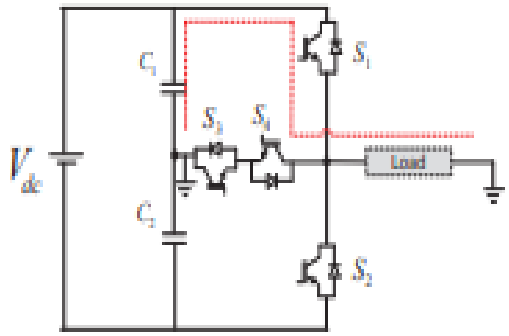
Fig. 2. Circuit schematic of the proposed architecture with a 1:5 asymmetry ratio

The auxiliary module runs at a greater switching frequency than the main bridge, which operates at almost fundamental frequency. The proposed topologies LDNs are self-balancing and keep the voltage of their capacitors at half of the matching bridge voltage. Capacitors supply auxiliary bridges, and closed loop management is necessary to maintain the appropriate capacitor voltage. It will ensure that the reference voltages fundamental component and the main module's fundamental ingredient align.

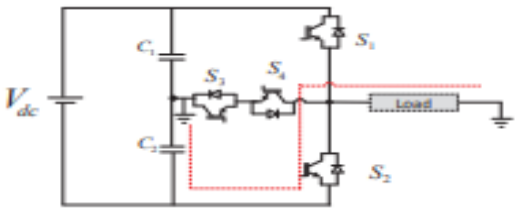
Capacitors C1 and C2 in Fig. 2(b) should keep their voltage at half of the DC link voltage. The present path and switching states for the three-level T-type Neutral Point Clamped Converter (TNPC) are shown in Fig. 3. When switch (S1) is activated and current flows through the top capacitor (C1), switch (S1) and load as indicated in Fig. 3(a), a positive voltage level can be reached. As shown in Fig. 3(b), a similar negative voltage level may be reached when current passes through the load, switch, and lower capacitor (C2). As indicated in Fig. 3(c), switches S3 and S4 will be switched ON to achieve the zero-voltage level. Table I displays the switching states of the primary bridge (TNPC). The capacitor balance of TNPC is challenging with LDN-based hybrid architecture. The upper and lower capacitors or C1 and C2, will have uneven charging and discharging periods in order to comply with the LDN concept.

TABLE 1. SWITCHING STATES OF TNPC

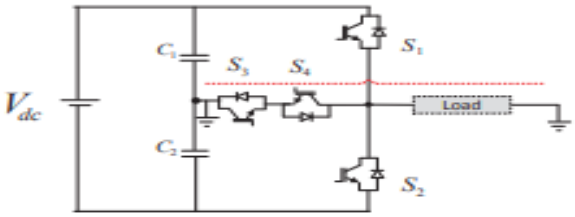
Levels	Sa	Sb	Sc	Sd	Phase voltage
Positive	1	0	0	0	Vdc/2
Zero	0	0	1	1	0
Negative	0	1	0	0	Vdc/2



(a)



(b)



(c)

Fig. 3. shows the present path and switching state for a three-level TNPC: (a) positive voltage level (b) negative voltage level and (c) zero voltage level.

LDN will operate in a negative half cycle in the proposed design. The lower dc bus capacitor in this setup will supply more power than the top dc bus. Consequently, the upper DC bus capacitor will continue to charge and the lower DC bus capacitor will continue to discharge over time. Eventually, the lower dc bus voltage will drop to zero in steady state as the higher dc bus absorbs the whole main dc bus voltage. Therefore, power must be pumped from the top capacitor to the lower capacitor in order to prevent this scenario. Additionally, in the event that the LDN receives power from the top DC bus capacitor, a power flow arrangement between lower capacitor C2 and higher capacitor C1 must be established. This is guaranteed by a second converter, whose rating is substantially lower than the primary converter's. Only one switch, one diode, and a low-value inductor were needed for this additional converter. However, by eliminating a large and costly transformer, this tiny rating converter aids in balancing the capacitor voltages of TNPC.

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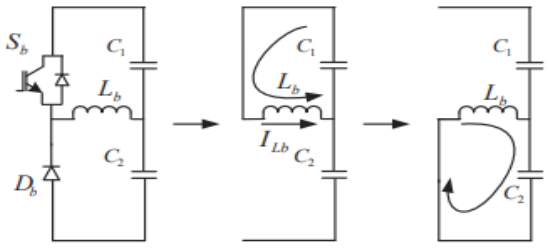

Fig. 4: An additional circuit to equalize the voltages of the capacitors (a) Schematic layout (b) Upper capacitor discharge stage (c) Lower capacitor charging stage.

One TNPC circuit is added in order to balance the voltage of the upper and lower capacitors; this additional circuit serves as the common circuit for all three phases. Fig. 4 shows the extra circuit and how it functions. As seen in Fig. 4(b), capacitor C1 will transmit its energy to inductor Lb when the voltage across it exceeds that across C2. This will cause switch Sb to be ON. The inductor causes diode Db to become forward biased when switch "Sb" is turned off, which lowers capacitor C2's charge from the inductor Lb, as shown in Fig. 4(c). In this manner, the voltages of the two capacitors will equalize and attain the target voltage in a steady state.

TNPC capacitor voltage balancing with closed-loop current control:

A closed loop control can be used to balance the upper and lower capacitors, C1 and C2, appropriately. A closed loop control block diagram is shown in Fig. 5 in order to balance the upper and lower capacitors. This control method uses two control loops to balance the voltage of the capacitor. The outer voltage loop and the inner current loop make up this control loop. In this diagram, VRef represents the necessary voltage and VC represents the voltage measured from the higher capacitor. To set the capacitor voltage to the appropriate value, the low gain PI controller receives the difference between the measured voltage and reference voltage. The purpose of the inner current loop is to lower both the beginning shoot-through current and current ripple. To produce a PWM signal that will aid in operating switch "Sb," the output of the second controller is compared to the carrier signal.

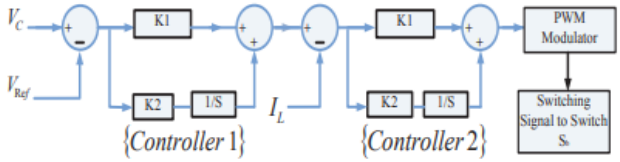

Fig.5 Block diagram of closed loop control to balance capacitor voltage.

2. SIMULATION RESULTS

MATLAB/Simulink is utilized to assess the hybrid asymmetrical multilevel inverter architecture with a 1:5 ratio. This simulation's primary objective is to evaluate how well TNPC works when combined with an extra converter to combine three phases and eliminate a transformer. Table II provides the simulation parameters.

TABLE 2. SIMULATION PARAMETERS

Parameters	Values
Voltage of main bridge	200V
Voltage of main LDN	100V
Voltage of Auxiliary bridge	40V
Voltage of Auxiliary LDN	20V
Maximum line to line Voltage (rms)	297.76V

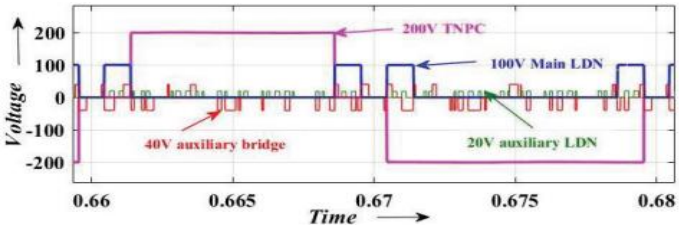

Fig.6 Voltage waveform of individual cells

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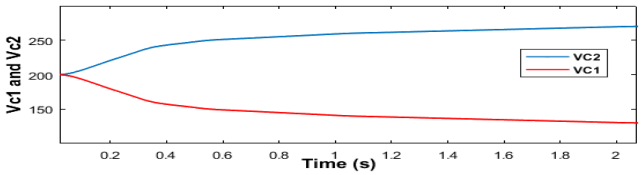

Fig.7 Voltage across upper and lower capacitor

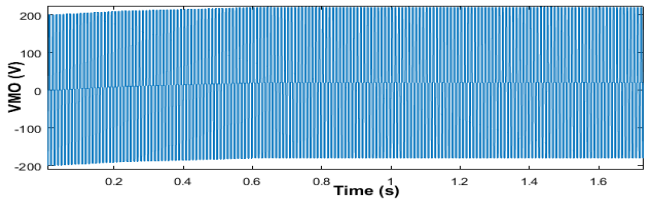

Fig.8 Output voltage across main bridge i.e. TNPC

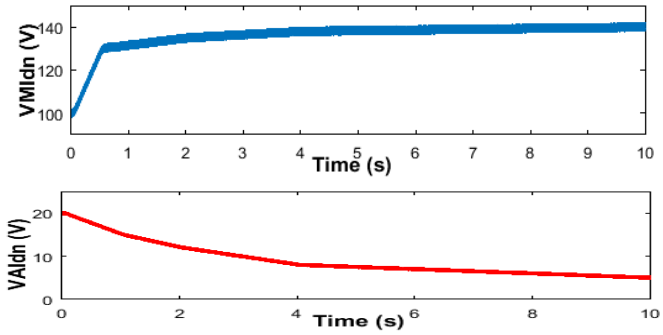

Fig.9 Voltage waveform across main LDN and auxiliary LDN capacitors

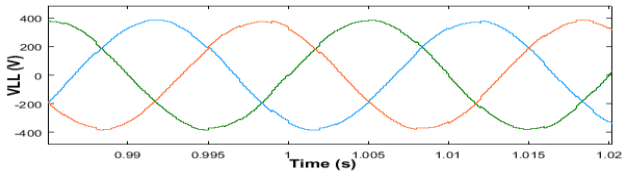

Fig. 10 Output line to line voltage

Auxiliary bridge, main LDN, main bridge, and auxiliary LDN output voltage waveforms are shown in Fig. 6. The resulting output phase voltage is composed of these waveforms overlaid. The basic switching frequency is where high voltage cells operate and the higher voltage cells operate at a higher frequency. In order to maximize conduction losses, it will be helpful to choose devices properly. In this section, the hybrid converter simulation outcomes with and without an extra converter to balance the capacitor voltages are described.

Case 1: Hybrid inverter with asymmetric features without extra converter

Initially the main bridge (TNPC) of the hybrid asymmetrical multilevel converter will be studied without the need for a second converter. Fig.7 to Fig.10 display the corresponding waveforms. Fig.7 depicts the capacitors C1 and C2 will continue to charge and discharge, respectively, until the voltage across C1 reaches the main DC bus voltage in a constant state. The deviation in capacitor voltage will have an impact on the TNPCs output. Additionally, there cannot be a perfect three-level output like in Fig. 8. The voltage between the main LDN and auxiliary LDN of the capacitor will deviate from the intended values of 100 V and 20 V, respectively, as shown in Fig. 9. The waveforms of the primary LDN and auxiliary LDN capacitors, which will continuously charge and discharge, are shown in the above illustration. The inverter is unable to provide voltage in equal steps because of the divergence in LDN voltage. Fig. 10 shows distorted line to line voltage.

Case 2: An extra converter and an asymmetric hybrid inverter

The performance of the converter is displayed from Fig. 11 to Fig. 16 when an extra converter is added with TNPC. The voltage across capacitors C1 and C2 stabilizes, as seen in Fig. 11. Fig. 12 illustrates the steady state voltage across both capacitors and the balancing of capacitors at the required voltage. Fig. 13 displays the three-level output voltage of the TNPC. The inductor current of an extra converter is shown in Fig. 14. Controller 2 helps to limit ripples in the inductor current. The rating of switch Sb will decrease with less variations in the inductor current. As seen in Fig. 15, this extra converter aids in maintaining the voltages of the LDN capacitors. Fig. 16 displays the balanced three level line to line voltage at unity modulation index.

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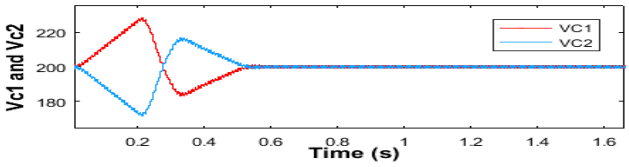

Fig. 11 Voltage across upper and lower capacitor

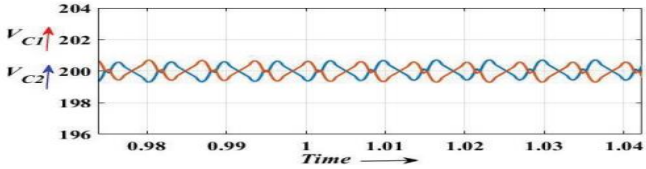

Fig.12 Steady state voltage across upper and lower capacitors

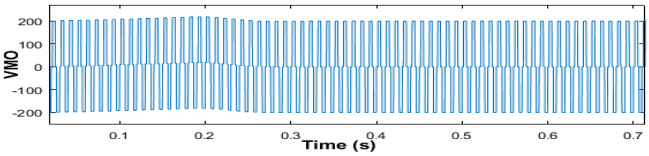

Fig.13 Three Level output voltage across TNPC

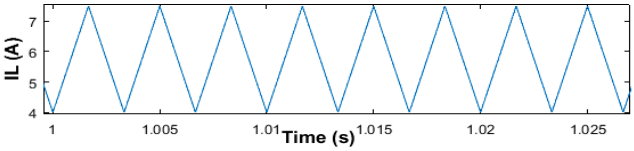

Fig. 14 Inductor current of additional converter

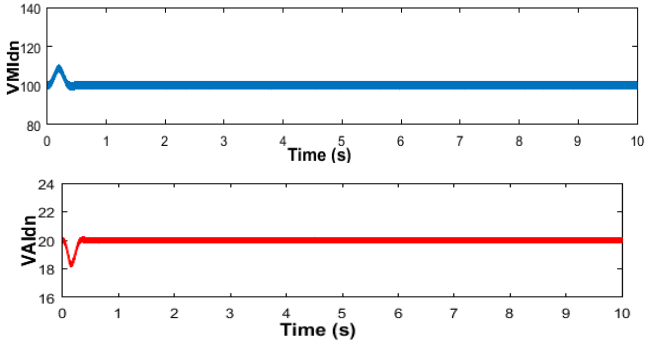

Fig.15 Voltage across main LDN and auxiliary LDN capacitors

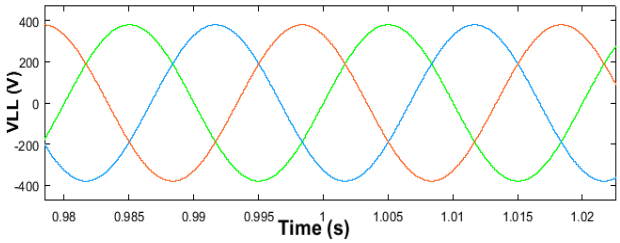

Fig.16 Output line to line voltage at unity modulation index

3. CONCLUSION

This study presents a proposal for a hybrid asymmetrical transformerless multilevel converter with one DC source, based on double LDN. The main bridges DC buses are combined and supplied by a single DC source. To eliminate the isolation transformer, three phase TNPC was used in place of the main bridges in the previous generation of high-resolution multilevel converters. The conversion rating of these transformers is complete. The suggested work uses a second converter to guarantee that the TNPC capacitors capacitor voltages are balanced. The rating of this extra non-isolated dc-dc converter is just 7–8% of the rating of the primary converter. To equalize the voltage across capacitors, a closed loop current controller is employed. By substituting the power frequency transformers, this additional converter is anticipated to lower installation and operating costs (losses) and boost system efficiency. 43 levels in the output voltage are obtained by using a total of 12 switches per phase and a single dc source for all three phases. Simulations using MATLAB/Simulink are used to confirm the suggested topologies performance.

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