INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)

e-ISSN : 2583-1062

Impact Factor : 5.725

www.ijprems.com
editor@ijprems.com

Vol. 03, Issue 10, October 2023, pp : 295-299

DESIGN OF DOUBLE DATA RATE SDRAM CONTROLLER

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ABSTRACT

SDRAM (synchronous dynamic RAM) memory is used in many applications like smart phones, laptops because of its reduced area, high speed, configurable and less latency and high performance and also it provides double data rate. It is important to maintain the memory refresh, read, write signals and initialize functions to implement the SDRAM memory by connecting proper signals. For this purpose the controller is designed which controls the SDRAM memory by predefined set of command signals. In this paper the optimized controller is designed and implemented on FPGA. And also the design has been focused on both read and writes operation at the same time to maintain the configurable latency.

Keywords – SDRAM, Less Latency, High Performance, FPGA.

1. INTRODUCTION

Synchronous DRAM (SDRAM) is implanted framework memory outline as a result of its pace and pipelining capacity. In top of the line applications, similarly chip will be particular implicit peripherals to give interface to the SDRAM. Be that as it may, for different applications, the framework planner must outline a particular memory controller to give order signs to memory revive, read and compose operation and instatement SDRAM.

In this paper, the SDRAM controller situated between the SDRAM and the transport expert, minimizes the push to manage the SDRAM memory by giving a straightforward framework to connect with the transport expert. Figure 1 is the piece chart of the DDR SDRAM. Memory Controller associated between the transport expert and SDRAM.

SDRAM's arrange in light of information exchange rates. In Single information rate SDRAM, information exchanged on each rising edge of the check though in twofold information rate (DDR) SDRAM's the information on each rising edge and each falling edge of the clock will transfer and accordingly the throughput is expanded. DDR SDRAM Controllers are speedier and proficient than its partners. They permit information exchange at a speedier rate without much increment in clock recurrence and transport width.

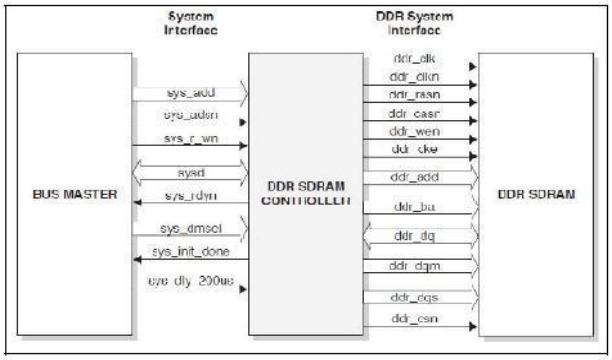

Figure 1: DDR SDRAM controller system

Same Commands as for Standard SDRAM

- READ
- WRITE
- ACTIVATE
- PRECHARGE
- REFRESH
- MRS (Mode Register Set)

Added

- EMRS (Extended MRS)
- Phase Shift the Data Strobe
- Resynchronize the Data

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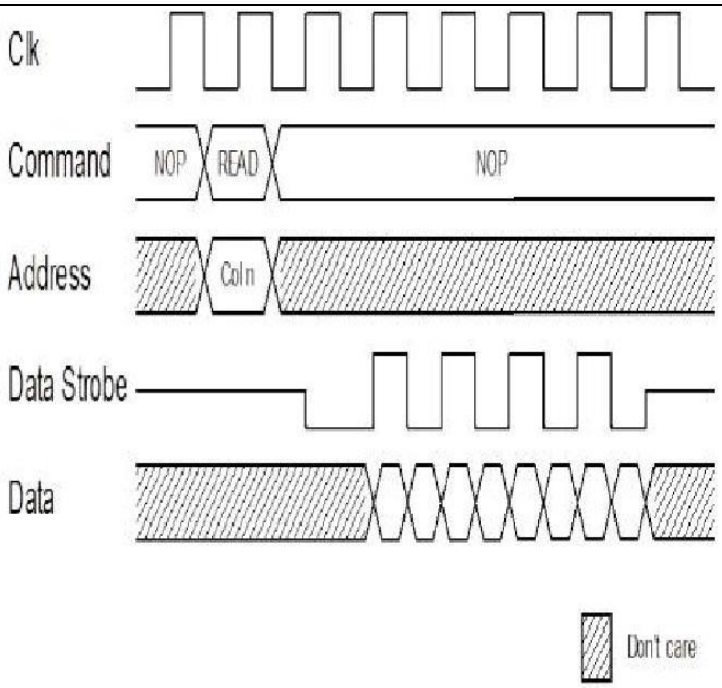

Figure 2: clock operation proposed methodology

DDR SDRAM Controller module gets addresses and control signals from the BUS Master. The Controller creates summon flags and these sign s the information will be perused or kept in touch with a specific memory area. The DDR SDRAM Controller design appeared in Figure 2.

It comprises of three modules:

1. Main control module
2. Signal era module
3. Information way module

The primary control module has two state machines and are vive counter. The two state machines are for instatement of the SDRAM and for creating the orders to the SDRAM. They produce iState and cState yields as indicated by the framework interface control signals. The sign era module now creates the location and order signals relying on the iState and cState e. The information way module plays out the read and compose operations between the transport expert and DDR. Taking after are a portion of the critical components of DDR SDRAM Controller:

- The DDR SDRAM Read and Write operations improved by the controller.
- For instating the DDR SDRAM controller, partitioned state machines composed inside.
- The entrance time for read and the compose cycle streamlined in view of the CAS inertness and burst length of the DDR SDRAM.
- The auto revive for the DDR SDRAM is finished by the controller.

The main control module consists of three sub modules:

1. Initialization FSM module (INIT_FSM).
2. Command FSM module (C MD_FSM)
3. Counter module

A. Main control module:

The DDR SDRAM Controller needs to experience an introduction procedure by an arrangement of order signs state LOAD MODE REGISTER order is produced to arrange the DDR SDRAM to a particular method of before the ordinary memory access. The introduction limited state machine in the principle control module is in charge of the instatement of the DDR SDRAM controller. Figure demonstrates the state outline of the introduction FSM (INIT_FS M). At whatever point reset sign is high, the instatement FSM will change to i_IDLE state. Once the reset signal goes low, the controller needs to sit tight for 200us clock adjustment delay. This continually checked by sys_ dly_200us signal and a high on the sys_dly_200us will demonstrate that the clock adjustment postponement is finished. The DDR instatement grouping will start promptly after the clock/power adjustment is finished and afterward the INIT_FSM will change its state from i_IDLE to i_NOP state. From the i_NOP state, the instatement FSM will change to the i_PRE state on the following clock cycle

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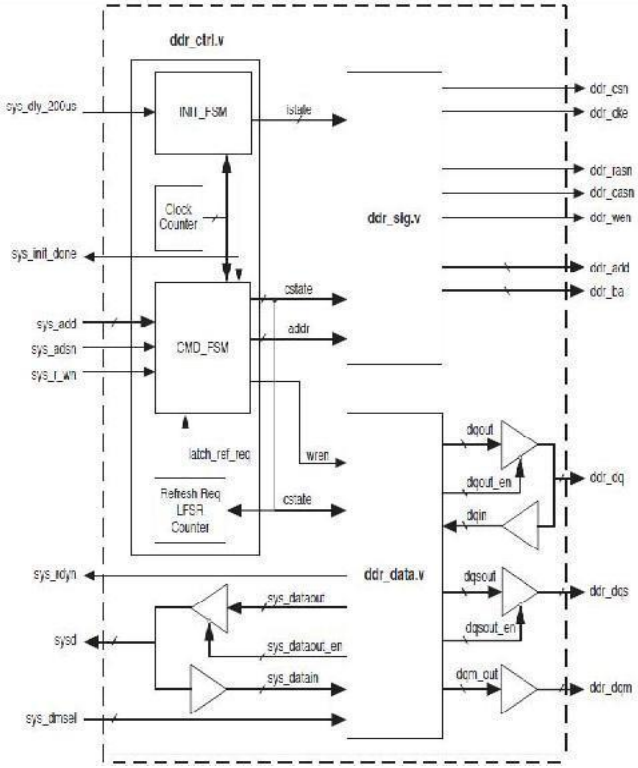

Figure 3: Functional block diagram of DDR SDRAM controller

In the i_PRE state, the fundamental control module will create the PRECHARG E order. The PRECHARGE order produced amid this state will be connected to every one of the banks in the gadget. Once the PRECHARGE charge is created by the introduction FSM, it will change to the following state. The following state in the outline of introduction FSM is two AUTO REFRESH charges. These revive charges are produced to invigorate the DRAM memory. After the two invigorate state, the instatement FSM will change to i_MRS state. Amid this operation.

In the wake of fulfilling the i_MRS timing delay the instatement FSM will change to i_ready state. The introduction FSM will stay in the i_ready state for typical memory access. Furthermore, when the introduction FSM changes to i_ready state signal sys_INIIT_DONE is set to high to show that DDR SDRAM controller in statement is finished. The i_PRE, i_AR1, i_AR2, i_EMRS and i_MRS states are utilized for issuing DDR summons. CMD_FSM handles the read, write and refresh of the SDRAM. The CMD_FSM state machine is initialized to c_IDLE during res set. After reset, CMD_FSM stays in c_IDLE as long as sys_INIT_DONE is low which indicates the SDRAM initialization sequence is not yet completed. When the sys_INIT_DONE is high, it indicates the system initialization is complete

2. SIMULATION RESULTS

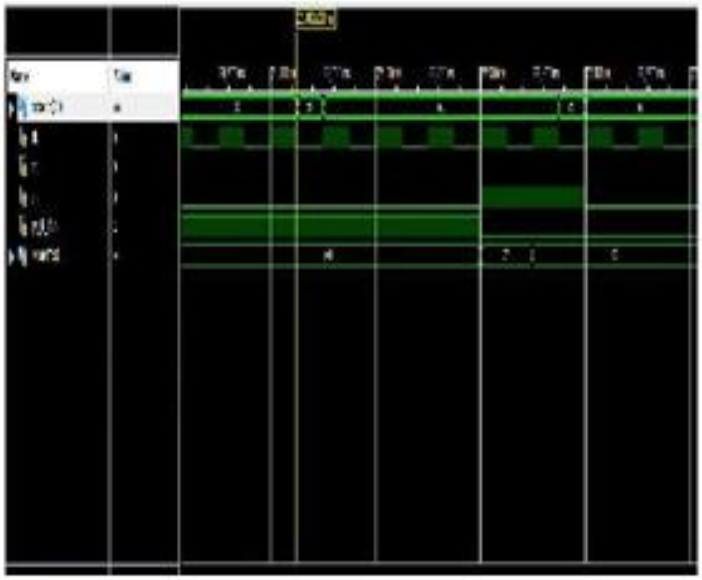

Figure 4: Simulation Waves of the proposed work

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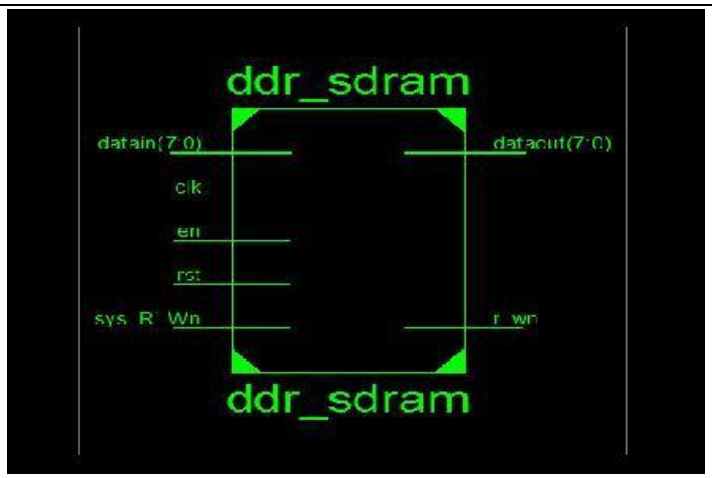

Figure 5: RTL Schematic Diagram for the Top module

The above simulation results shows the data synchronization between input and output data with respective to the proposed algorithm mentioned with SYS_R_Wn signal which is responsible for the synchronization with respective to the clock signal. We can observe that the data input as e1 could be coming as output after the synch_r_wn signal is been trigger with respective clock frequency.

The controller will now sit tight for latch_ref_req, sys_INIT_DONE flags and will enter auto revive, read and compose mode relying on these signs. At the point when the instatement is finished and when the latch_ref_req goes high the controller will revive by going into invigorate state. After the revive is finished, when the latch_ref_req and sys_ADSn signal goes low, the controller will go to dynamic state. The ACTIVE summon will be issued for every reused or compose access to open the column.

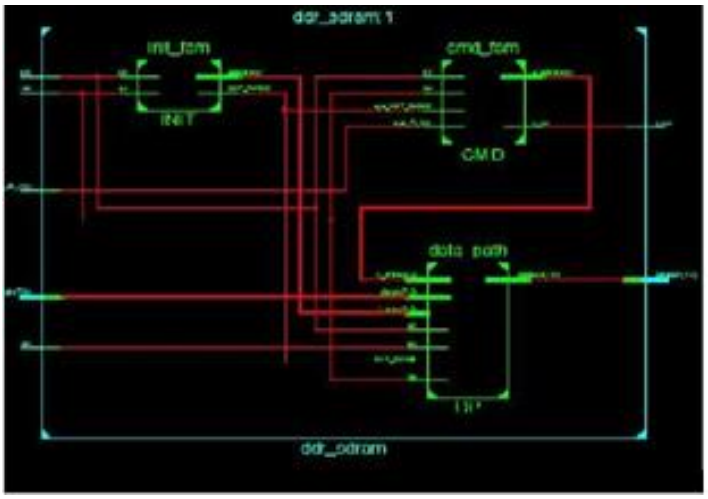

Figure 6: RTL Schematic Diagram for the Top module in brief view

Figure 7: Technology Schematic Diagram for the Top module

3. CONCLUSION

It was concluded that we can transmit data by using rising edge and falling edge. The time taken to transmit data is in the order of nanoseconds. The DDR SDRAM Controller architecture is implemented in Verilog HDL. The RTL Simulation results are obtained using Verilog HDL. When reset goes to high the Initialization of DDR SDRAM will be started it has to wait 200µs.It will be indicated with the help of INT_DONE goes to low. When reset goes to low the Initialization of DDR SDRAM is finished i.e. INT_DONE goes to high. If enout_write is low the write operation is in progress and enout_write is high the write operation is completed. When enable is low and reset is low the DDR SDRAM memory controller completed the read operation then enout_read goes to high.

4. FUTURESCOPE

In future the time taken for initialization of DDR SDRAM memory controller is 200µs. That time can be reduced to improve the fast operation on read and write cycle. To improve the efficiency of such a system the Data Buffers would need to be larger but that would increase the core size of the Memory Controller. A caching system for such a system has to be evaluated with respect of performance gain compared to the extra cost for the larger memories. The largest gain with a caching system would be when the bursts are short and to consecutive locations in conjunction with using a default burst length of eight.

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