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OPTIMIZED HIGH-SPEED AND AREA-EFFICIENT VLSI ARCHITECTURE FOR THREE-OPERAND BINARY ADDERS

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ABSTRACT

Arithmetic and logic unit has been the most significant unit in any electronic devices. In the recent advancement, for an arithmetic and logic unit to be significant it needs to have an efficient algorithmic operation such as Multiplications and addition. Three- operand binary adder is the basic functionalunit to perform the modular arithmetic in various cryptography and pseudorandom bit generator (PRBG) algorithms. A parallel prefix two-operand adder such as Han-Carlson (HCA)can be used for three-operand addition that significantly reduces the critical path delay at the cost of additional hardware. This paper presents Low power and high Speed three inputBinary Adder. Project will be developed using Verilog HDL. Xilinx ISE tool is used to perform the Simulation and Synthesis. The simulation results of presented adder will represent that it will have less power dissipation, lesser area and less delay compared to Carry save adder (CS3A).

Keywords: carry save adder (CSA), Han- Carlson adder (HCA), Three input adder, Arithmetic and logic unit.

1. INTRODUCTION

Digital systems are highly complex at their most detailed level. They may consist of millions of elements i.e., transistors or logic gates. For many decades, logic schematics served as thengua. Franca of logic design, but not anymore. Today, hardware complexityhas grown to such a degree that a schematic with logic gates is almostuseless as it shows only a web of connectivity and not functionality of design. Since the 1970s, computer engineers, electrical engineers and electronics engineers have moved toward Hardware description language (HDLs). Digital circuit has rapidly evolved overthe last twenty five years [1].

The earliest digital circuits were designed with vacuum tubes and transistors. Integrated circuits were then invented where logic gates were placed on a single chip. The first IC chip was small scaleintegration (SSI) chips where the gate count is small. When technology became sophisticated, designers were able to placecircuits with hundreds of gates on a chip [2]. These chips were called MSI chips with advent of LSI; designers could put thousands of gates on a single chip. At this point, design process is getting complicated and designers felt the need to automate these processes.

With the advent of VLSI technology, designers could design single chip withmore than hundred thousand gates. Because of the complexity of these circuits computer aided techniquesbecame critical for verification and for designing these digital circuits [3]. Oneway to lead with increasing complexity of electronic systems and the increasing timeto market is to design at high levels of abstraction. They are used forspecification, simulation and synthesis of an electronic system. This helps to reduce the complexity in designing and products are made to be available in market quickly. The components of a digital system can be classified as being specific to an application or as being standard circuits.

To achieve optimal system performance while maintaining physical security, it is necessary to implement the cryptography algorithms on hardware. Modular arithmetic such as modular

exponentiation, modular multiplication and modular addition is frequently used for the arithmetic operations in various cryptography algorithms. Therefore, the performance of the cryptography algorithm depends on the efficient implementation of the congruentialmodular arithmetic operation. The mostefficient approach to implement the modular multiplication and exponentiationis the Montgomery algorithm whose critical operation is based on three- operand binary addition is also a primary arithmetic operation in the linear congruential generator (LCG) based pseudo-random bit generators (PRBG)[4].

The three-operand binary addition can be carried out either by using two two- operand adders or one three-operand adder. Carry-save adder (CS3A) is the area-efficient and widely adopted technique to perform the three-operand binary addition in the modular arithmetic used in cryptography algorithms and PRBG methods. However, the longercarry propagation delay in the ripple-carrystage of CS3A seriously influences the performance of the MDCLCG (Modified dual coupled linear congruential generator) and other cryptography architectures on IoT based hardware devices [5].

In order to shorten the critical path delay, a parallel prefixed twooperand adder such as Han-Carlson (HCA) can also be used for three-operand binary addition. It reduces the critical path delay but increases the area. Therefore, it is necessary to develop an efficient VLSI architecture to carry out the fast three- operand binary addition with minimum hardware resources.

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2. LITERATURE SURVEY

M. M. Islam, M. S. Hossain, M. K. Hasan,

M. Shahjalal, and Y. M. Jang, et. al. [6] presents FPGA implementation of high-speed area-efficient processor for elliptic curve point multiplication over primefield. Elliptic Curve Cryptography (ECC) has recognized much more attention over the last few years and has time-honored itself among the renowned public key cryptography schemes. The performance of hardware implementation for ECC is affected by basic design elements such as a coordinate system, modular arithmeticalgorithms, implementation target, andunderlying finite fields. This paper shows the generic structure of the ECC system implementation which allows the differenttypes of designing parameters like elliptic curve, Galois prime finite field GF(p), andinput type. The ECC system is analyzed with performance parameters such asrequired memory, elapsed time, and process complexity on the MATLABplatform.

K. Panda et. al. [7] presents a modified Montgomery modular radix-2 iterative multiplier for the effective implementation of 1024-bit BBS (BlumBlum Shub) generator hardware. The BBSeffective implementation technique depends on the larger integer multiplication that can make it ascomputationally expensive. The two- operand adders are replaced with three-operand adders by this approach. For three-operand addition, most generallyutilized adder is CSA that can experience the higher critical path delays. The results of this 1024-bit BBS implementation isoperates at high frequency (71.2 MHz) and achieved improvement in latency.

Z. Liu, J. GroBschadl, Z. Hu, K. Jarvinen,

H. Wang, and I. Verbauwhede, et. al. [8] presents Elliptic curve cryptography with efficiently computable endomorphisms and its hardware implementations for the Internet of Things. In this work, we study

the computation of this operation on a twisted Edwards curve with an efficiently computable enmorphism, which allows reducing the number of point doublingsby approximately 50 percent compared to a conventional implementation. We develop several optimizations to the operation and we describe two hardware architectures for computing the operation. Our designs offer various trade-offs and optimizations between performance and resource requirements and they are valuable for IoT applications.

Z. Liu, D. Liu, and X. Zou, et. al. [9]presents An efficient and flexible hardware implementation of the dual-fieldelliptic curve cryptographic processor. This paper presents field-programmable gate array (FPGA) implementation of ahigh-speed, low-area, side-channel attacks(SCAs) resistant ECC processor over a prime field. The paper proposes novel hardware architectures for point addition and point doubling operations on the twisted Edwards curve, where the processor takes only 516 and 1029 clock cycles to perform each point addition and point doubling, respectively. The implemented design is time-area-efficient as it offers fast scalar multiplication with low hardware utilization without compromising the security level.

S.-R. Kuang, et. al. [10] presents a multiplication method using Montgomery Modular to perform modular multiplication very quickly. The Montgomery Modular (MM)multiplication can be utilized in the process of encryption using PKC (Public Key Cryptography). The MM with larger integers consumes huge time in PKC. Hence several algorithms are presented for performing MM very fast and Montgomery's algorithm is one among them. This approach replaced the complicated divisions in MM with sequence of modular shifting additions. The Montgomery algorithm is divided in to two types depends on input and output operands representation. The two types are SCS-MM (Semi- Carry-Save Montgomery modular Multiplication) and FCS-MM (Full Carry-Save MM). This technique uses carry save adder for multiplication process. This carry save addition increases critical path delay.

3. THREE OPERAND BINARYADDER

The three-operand binary addition is one of the critical arithmetic operations in the congruential modular arithmetic architectures. Carry-save adder (CSA) is the commonly used technique to perform the three-operand binary addition. It computes the addition of three operands intwo stages. The first stage is the array of full adders. Each full adder computes "carry" bit and "sum" bit concurrently from three binary input ai,bi and ci. The second stage is the ripple-carry adder that computes the final n-bit size "sum" and one-bit size "carry-out" signals at the output of three-operand addition. The "carry-out" signal is propagated through the n number of full adders in the ripple- carry stage. Therefore, the delay increases linearly with the increase of bit length. The architecture of the three-operandcarry-save adder is shown in Fig.1 shows the critical path delay depends on the carry propagation delay of ripple carry stage.



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Fig 1: THREE OPERAND CARRY SAVEADDER (CS3A)

The major drawback of the CS3A Adderis largest critical path delay which

increases with an increase of bit length. This critical propagation path delay influences the overall latency of the congruential modular arithmetic-basedcryptography and PRBG architectures.Hence, to shorten the critical path delay, two stages of parallel prefix two-operand adder can also be used. The Han-Carlson adder provides a reasonably good speed atlow gate complexity.

Thus, the three-operand addition can be performed using Han-Carlson adder (HCA) in two stages, as shown in Fig. 2. The maximum combinational path delayof HC3A depends on the propagate chain.





The HCA-based three-operand binary adder (HC3A) greatly reduces the critical path delay in comparison with the threeoperand carry-save binary adder. However, the area increases with increase of bit length. Therefore, to minimize this trade-off between area and delay, a new highspeed, area-efficient three-operand adder technique and its efficient VLSI architecture is proposed.

The proposed VLSI architecture of the three-operand binary adder and its internal structure is shown in Fig. 3. The new adder technique performs the addition of three n-bit binary inputs in four different stages. The proposed adder technique is a parallel prefix adder. However, it has fourstage structures instead three-stage structures in prefix adder to compute the addition of three binary input operands such as bit-addition logic, base logic, PG (propagate and generate) logic and sumlogic.



Fig. 3: FIRST ORDER VLSI ARCHITECTURE OF PROPOSED THREE-OPERAND ADDER

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The logical expressions of all these four stages are defined as follows:

In the first stage (bit-addition logic), the bitwise addition of three n-bit binary inputoperands is performed with the array of full adders, and each full adder computes "sum (Si)" and "carry (cyi)" signals. The logical expressions for computing sum (Si) and carry (cyi) signals are defined in Stage-1.

Stage-1: Bit Addition Logic:

 $S_i = ai_bi_ci$,

 $cyi = ai \cdot bi + bi \cdot ci + ci \cdot ai$

In the first stage, the output signal "sum (Si)" bit of current full adder and the output signal "carry" bit of its rightadjacent full adder are used together tocompute the generate (Gi) and propagate (Pi) signals in the second stage (base logic). The computation of Gi and Pi signals are represented by the "squaredsaltire-cell" as shown as:

Stage-2: Base Logic:

Gi:i = Gi = $S_i \cdot cyi-1$, G0:0 = G0 = $S_0 \cdot Cin$

 $Pi:i = Pi = S_i cyi-1, P0:0 = P0 = S_0 Cin$

The third stage is the carry computation stage called "generate and propagate logic" (PG) to precompute the carry bit and is the combination of black and grey cell logics. The logical diagram of black and grey cell is shown below:

Stage-3: PG (Generate and Propagate)Logic:

Gi: $j = Gi:k + Pi:k \cdot Gk-1: j$, Pi: $j = Pi:k \cdot Pk-1: j$

The final stage is represented as sum logicin which the "sum (Si)" bits are computed from the carry generate Gi: j and carry propagate Pi bits using the logical expression,

Stage-4: Sum Logic:

Si = (Pi _ Gi-1:0), S0 = P0, Cout = Gn:0

4. RESULT ANALYSIS

This section evaluates the performance of the proposed three-operand adder and shows the simulation results. For the implementation of this project the software tool required is Xilinx ISE 14.7. The simulation and synthesis results are executed by using Xilinx ISE14.7 This project uses the spartan3e for synthesis of the design. The code is developed using the Verilog HDL Language.



Fig. 4: BLOCK DIAGRAM OF PROPOSEDSYSTEM



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Fig. 5: RTL SCHEMATIC



Fig. 6: OUTPUT WAVE FORM

Fig. 6 shows the output waveform of proposed adder where we performed addition of 16 bit input data of a b c and cin and gives the output is 16 bit sum.

The properties of physical synthesis analysis are compromised with maximum combinational gate delay, consumption of area, Power, ADP, PDP are represented inTable 1.

Parameters	CS3A	НСЗА	
Delay (ns)	2.12	0.80	
Power μW	94.89	70.85	
Area μm^2	829.16	139.01	
Area X Delay (µm ² X ns) (ADP)	1757.82	788.79	
Power X Delay (µW X ns) (PDP)	107.38	48.18	

Table 1: COMPARATIVE ANALYSIS





Fig. 7: AREA-DELAY PRODUCT (ADP

times faster than the corresponding CS3A adder architecture. It is also worth noting that the proposed adder has significantly less ADP and PDP compared to CS3Aadder. This can be concluded that this adder is significantly better in terms ofdelay and power compared to other adders.





Implementation of the described Lowpower and high Speed three input Binary Adder represents that described method acquires less power, less area and less delay which automatically increases thespeed. ADP and PDP plots are represented in Fig. 7 and Fig. 8 respectively.

5. CONCLUSION

In this paper, Low power and high Speed three input Binary Adder is described. A parallel prefix two-operand adder such as Han-Carlson (HCA) can be used for three-operand addition. The proposed three-operand adder technique is a parallel prefix adder that uses four-stage structures to compute the addition of three input operands. For the implementation of this project the software tool required is XilinxISE 14.7. The code is developed using the Verilog HDL Language. From the physical synthesis results, this is clear that the proposed adder architecture is 3 to 9

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