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INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)
(Int Peer Reviewed Journal)
Vol. 04, Issue 08, August 2024, pp : 1010-1018

e-ISSN : 2583-1062
Impact Factor : 5.725

ENHANCED POWER EFFICIENCY IN 4-BIT EXCESS-3 TO BCD CONVERTERS USING ALTERNATIVE ONOFIC

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DOI: https://www.doi.org/10.58257/IJPREMS35861

ABSTRACT

In the real time of deep submicron circuits, low power consumption, compact chip size, and efficient performance are essential parameters. Striking a balance between these factors, particularly power reduction and high speed, presents a critical challenge. The emerging alternative ONOFIC technique demonstrates promise in addressing this challenge, offering significant power savings in the design of CMOS logic circuits. In this work, we propose a 4-bit excess-3 to BCD code converter utilizing this alternative ONOFIC approach and compare its performance against existing techniques like ONOFIC and stack ONOFIC.

1. INTRODUCTION

Deep submicron (DSM) integrated circuit (IC) [4] design demands low power consumption, making it a thriving research area. As technology advances, designs capable of achieving both low power and high-speed gain favor in DSM due to their efficiency. Digital arithmetic plays a crucial role in digital processors, signal processing, and communications, impacting factors like computation speed, processing time, system efficiency, and data throughput.

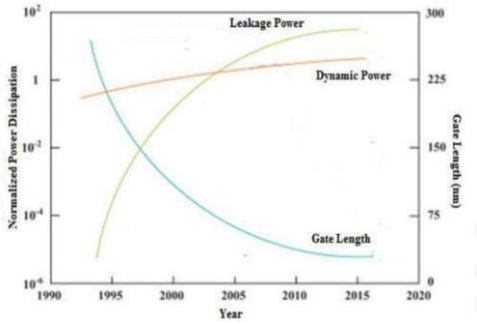

Fig.1. Trend, emphasizing the growing importance of leakage reduction with Shrinking gate lengths

However, low-power circuit design faces a three- dimensional challenge: Balancing chip area, power dissipation, and performance. In DSM, shrinking device dimensions reduces chip area for logic circuits, but reliability demands reduced supply voltage. While lowering supply voltage controls power consumption, it degrades performance without proportionally scaling down the threshold voltage. Balancing these factors is key. New technologies often increase power dissipation in ICs. Fig.1 showcases this trend, emphasizing the growing importance of leakage reduction with shrinking gate lengths. A skilled designer prioritizes efficient leakage reduction techniques in DSM. This paper proposes the "Alternate On/Off Logic (ONOFIC)" approach, a novel method for designing high-performance, low-power CMOS circuits

Leakage power [3] dissipation plagues both active and standby modes of CMOS circuits, making leakage [2] reduction crucial in deep submicron technologies [6]. Several established techniques address this challenge, offering various trade-offs and limitations.

Multi-Threshold CMOS (MTCMOS) utilizes virtual power rails controlled by high-threshold sleep transistors [1]. While effective in standby mode, it increases chip area and requires multiple mask layers [2].

Stacked Transistors: Connecting off-state transistors in series augments path resistance and reduces leakage [3]. However, this adds area and delays [4].

Sleep-Clocked CMOS (SCCMOS) turns off transistors connecting the main circuit to power in standby mode [5]. While effective, it necessitates a charge pump circuit, incurring area, power, and delay overheads [6].

Forced Stacking with MTCMOS: Combining these techniques tackles active and standby leakage but incurs area penalty and demands sleep signal management [7].

Leakage Control Transistors (LECTOR): This simple, single-threshold design employs two transistors to block leakage paths [8].

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Force Stacking with Additional High-Threshold Transistors: This reduces leakage by lengthening the leakage path but suffers from reduced output voltage swing and complex implementation [9].

Triple Sleep Transistors: Employing two regular and one high-threshold transistor to break leakage paths, this technique requires a controller for standby operation [10]. Power dissipation is a major problem [7] in microelectronic circuit designing the exclusively in wireless mobile applications and gadgets computing elements. This paper deals with the reduction and optimization techniques for leakage power reduction in VLSI CMOS circuits.

The causes of power dissipation in CMOS circuits are described by the given below equation.

$$P=1/2.C.VDD2.\ f.\ N+1\ leak.\ VDD+QSC.\ VDD.\ f.\ N \quad \text{.....(1)}$$

Where P signifies the total power dissipated. VDD represents the supply voltage, and f represents the operating frequency. The first term denotes the power required for charging and discharging the circuit nodes C is the node Capacitance. The factor N is the switching action which gives the number of gate transistors per clock cycle at the output. The second term in equation signifies the power dissipation due to the leakage current leakage. The term QSC shows the amount of charge carried during each transition by the short current in the circuit.

Selecting the most suitable leakage reduction technique hinges on specific design constraints and leakage reduction priorities. Carefully consider the potential drawbacks and trade-offs of each approach to find the optimal solution for your needs.

2. ONOFIC TECHNIQUE

The On/Off Logic (ONOFIC) approach offers a single-threshold voltage solution for reducing leakage current and power in CMOS circuits. It effectively decreases leakage in both active and standby modes by introducing an extra logic block between the pull-up and pull-down networks. This block, consisting of one PMOS and one NMOS transistor, operates in either 'on' or 'off' states, hence the name ONOFIC.

In Fig.2 the PMOS drain connects to the NMOS gate, the output connects to the NMOS source, and the PMOS source connects to the circuit's VDD. The NMOS drain connects to the circuit output and its source to ground, while the PMOS source connects to VDD. The ONOFIC block's functionality relies on this "on/off" property.

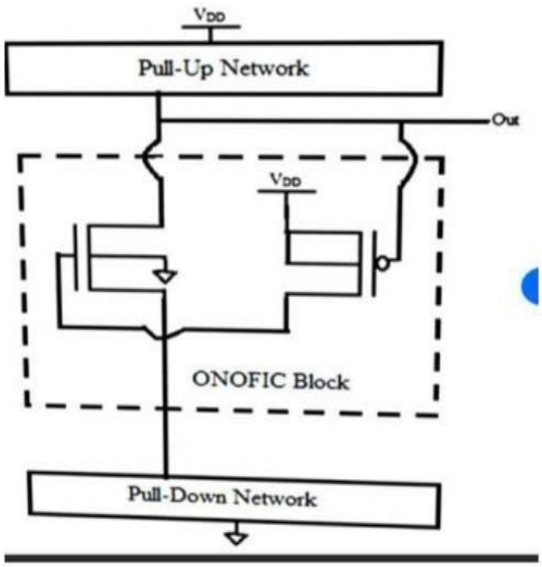

Fig.2. ONOFIC logic diagram

When the ONOFIC logic is 'on,' both transistors operate in the linear region, creating good conducting paths. Conversely, in the 'off' state, both transistors are cut-off, offering high resistance to control leakage current. This technique borrows the "force stacking" concept to achieve minimal resistance in the 'on' state and maximum resistance in the 'off' state. Importantly, the PMOS transistor governs the NMOS operation. Depending on the output logic, the ONOFIC NMOS and PMOS transistors must be in either cut-off or linear mode.

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A. Stack ONOFIC technique

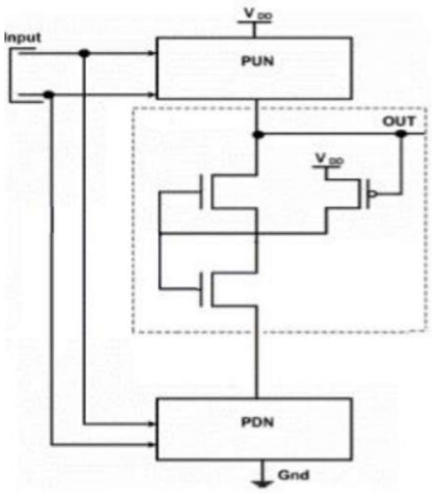

Fig.3. Stack ONOFIC logic diagram

As shown in Fig.3 tackles leakage power reduction in CMOS circuits using a singlethreshold voltage approach. Its name reflects the "on" and "off" states of its logic block, crucial for any output condition. This technique stacks two NMOS transistors controlled by a single PMOS transistor. When the PMOS is "on," both NMOS transistors enter the linear region, creating a low-resistance path for the circuit's output. This effectively reduces leakage current by minimizing unwanted leakage paths. Conversely, when the PMOS is "off," both NMOS transistors are driven into the cut-off region, exhibiting high resistance and significantly curbing leakage current. This "stacking" of off transistors further enhances leakage control compared to the single ONOFIC approach. Essentially, the PMOS acts as a switch, determining the state of the NMOS transistors and consequently the leakage current flow. This single-threshold design offers a simpler implementation compared to multithreshold techniques while effectively reducing leakage in both active and standby modes.

3. ALTERNATE ONOFIC TECHNIQUE

The Alternate ONOFIC approach, using two single- threshold ONOFIC blocks (one for pull-up, one for pull- down), tackles leakage power reduction in CMOS circuits. Each block has two transistors (NMOS and PMOS) and operates in either "on" or "off" states, minimizing leakage by blocking unwanted paths.

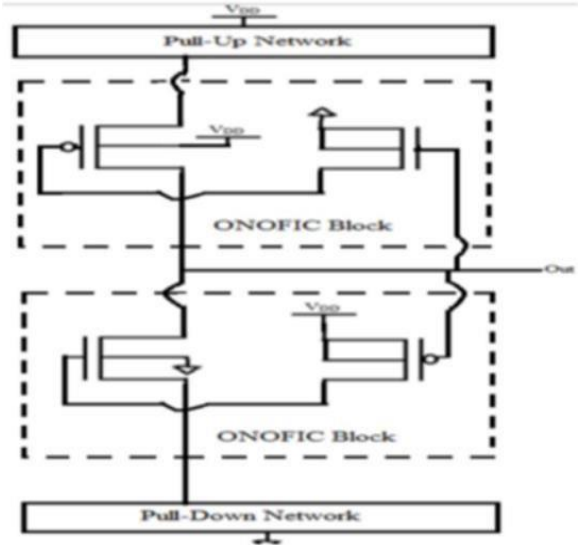

Fig.4. Alternate ONOFIC Technique

In a logic low output, the lower ONOFIC block conducts, creating a path from output to ground. Conversely, for a logic high output, the upper block conducts, connecting the output to the power supply. This "alternate" switching ensures only one path is active at a time, significantly reducing leakage. Path transistors (between output and network) handle current flow, while forced transistors (connected to output and controlling path transistor inputs) dictate their operation. Careful management of forced transistor inputs keeps leakage low while maintaining acceptable propagation delay.

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Voltage	Proposed ONOFIC technique	Stack ONOFIC technique	ONOFIC technique
5V	0.0323 µW	0.172 µW	0.226 µW
2.5V	0.0282 µW	0.0279 µW	0.0392 µW
1.5V	0.00936 µW	0.0725 µW	0.0189 µW

Table.1. Comparison of average power consumption in ONOFIC, Stack ONOFIC and Alternative ONOFIC technique for inverter

4. EXCESS-3 TO BCD CODE CON

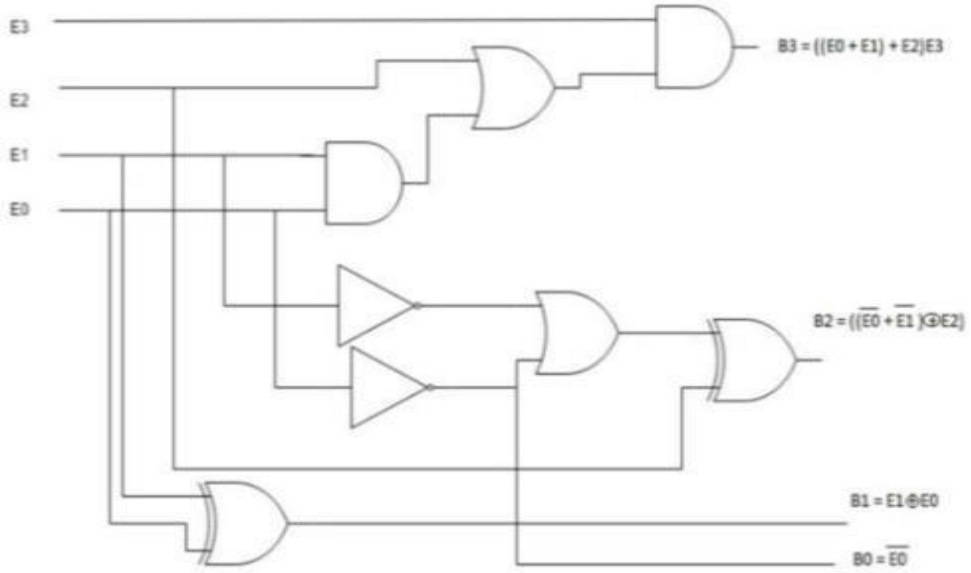

Fig.5. Excess-3 to BCD code converter

Digital circuits often require converting information between different codes for efficient processing. Code converters, as combinational circuits, play a crucial role in such conversions.

EXCESS-3 INPUT				BCD OUTPUT			
E3	E2	E1	E0	B3	B2	B1	B0
0	0	0	0	X	X	X	X
0	0	0	1	X	X	X	X
0	0	1	0	X	X	X	X
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

Table 2. Excess-3 to BCD code converter truth table

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5. SIMULATION RESULTS

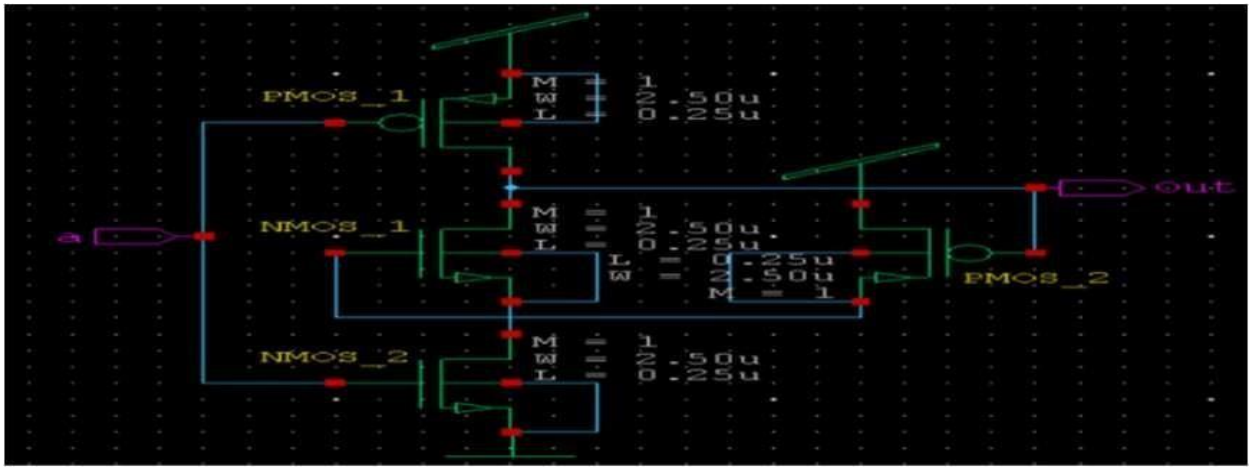

Fig.6. ONOFIC inverter

Fig-6 Explains is a **single-stage** ONOFIC **inverter**. This is a fundamental building block in digital electronics, responsible for inverting an input signal (0 becomes 1, and vice versa).

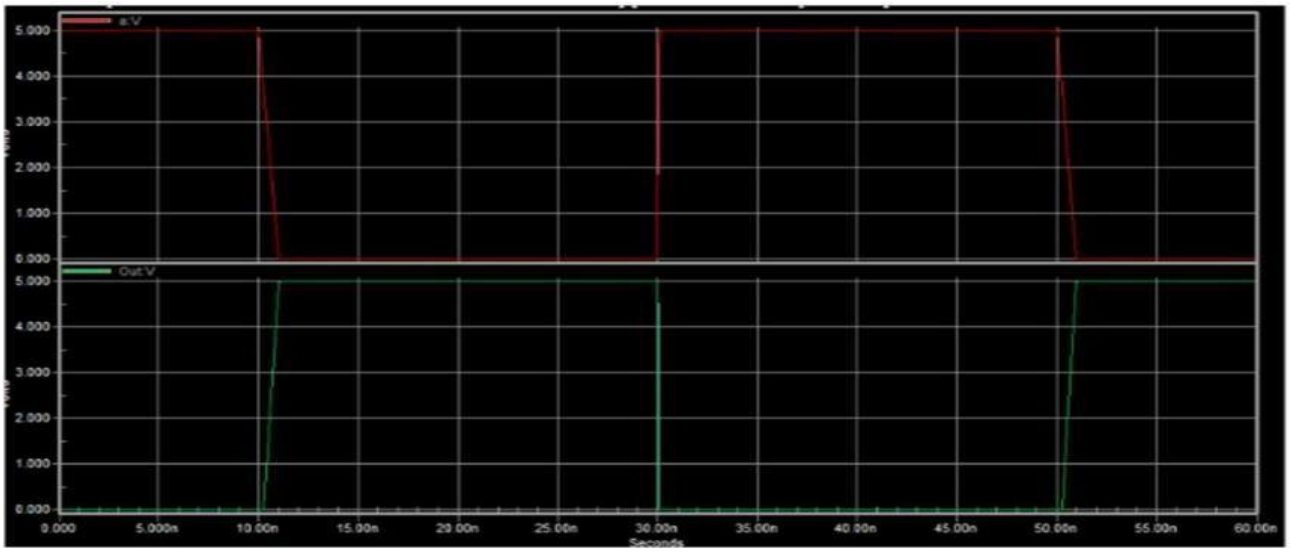

Fig.7. ONOFIC inverter-circuit and waveform Stack ONOFIC inverter

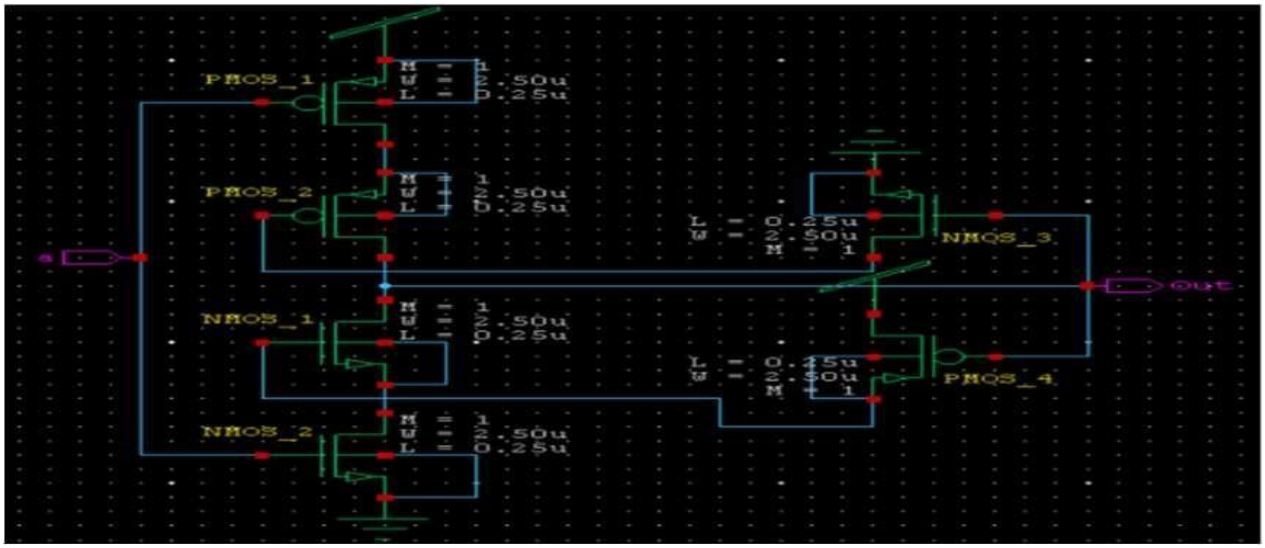

Fig.8. Stack ONOFIC inverter

Figure-8- Explains When the input is low, NMOS_1 is off, and PMOS_1 is on, pulling the output high. When the input is high, NMOS_1 is on, and PMOS_1 is off, pulling the output low.

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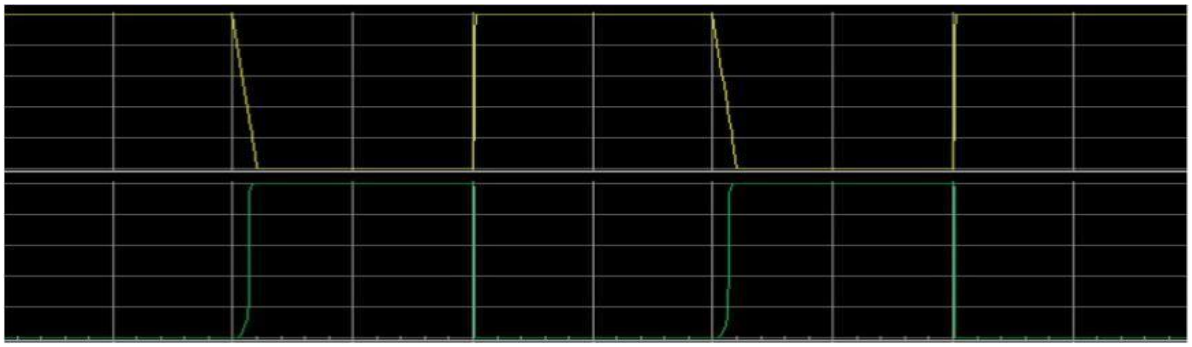

Fig.9. Stack ONOFIC inverter-circuit and waveform

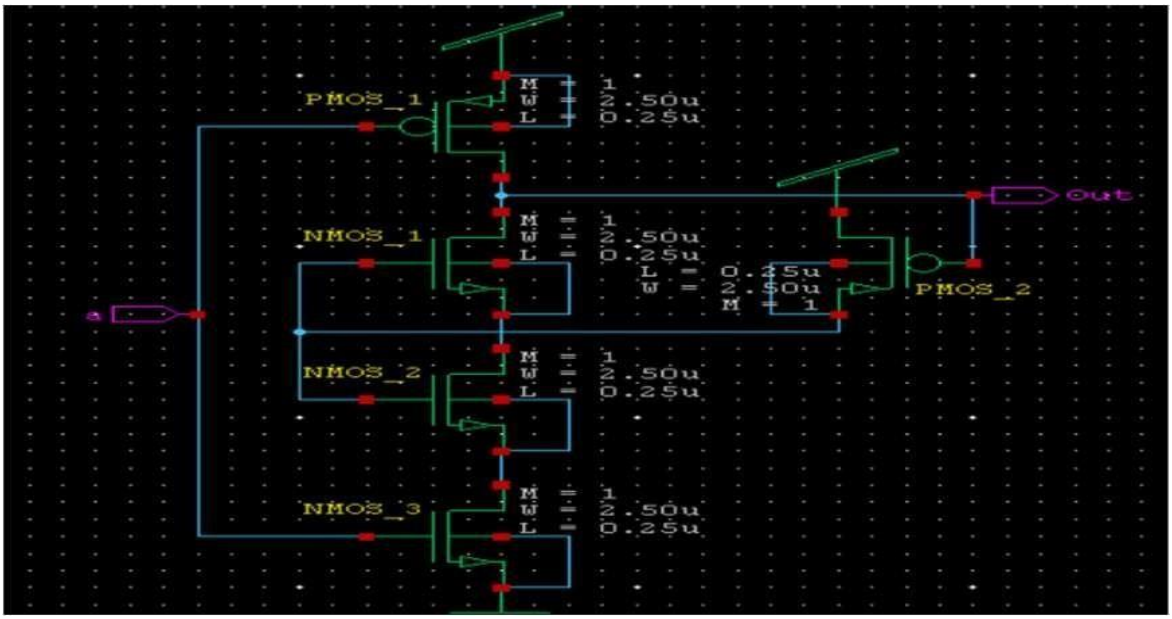

Fig.10. Alternative ONOFIC inverter

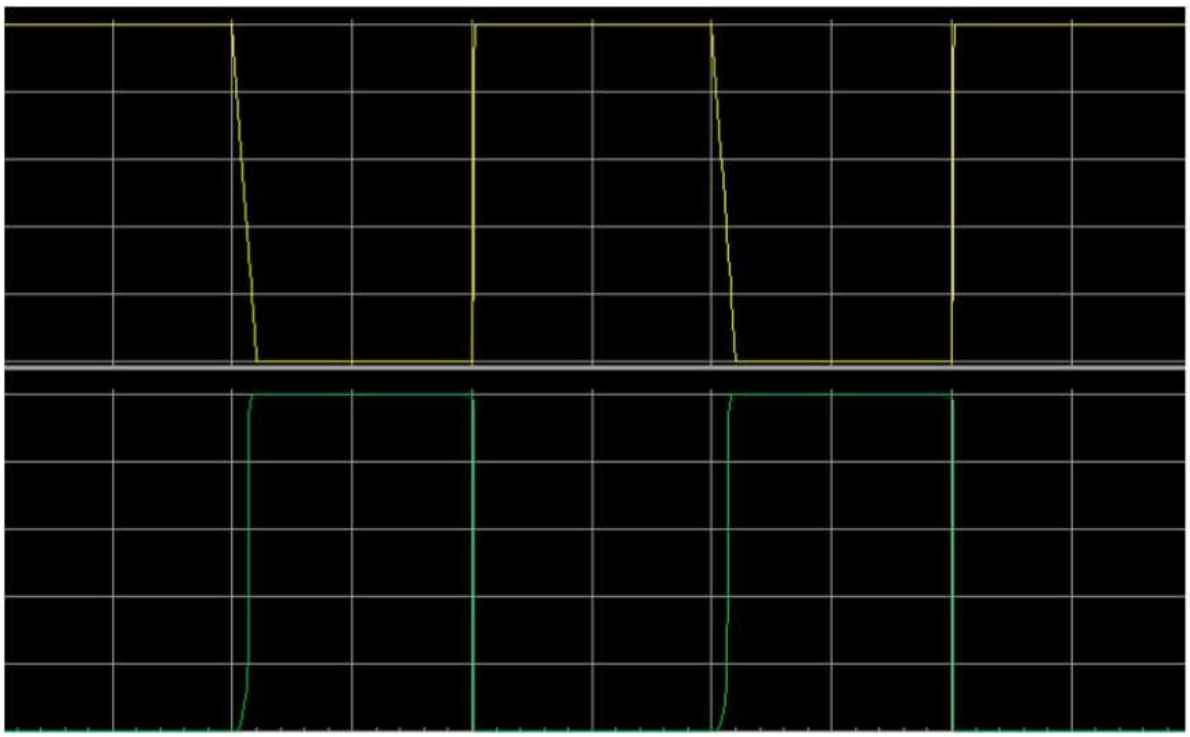

Fig.11. Alternate ONOFIC inverter –circuit and waveform

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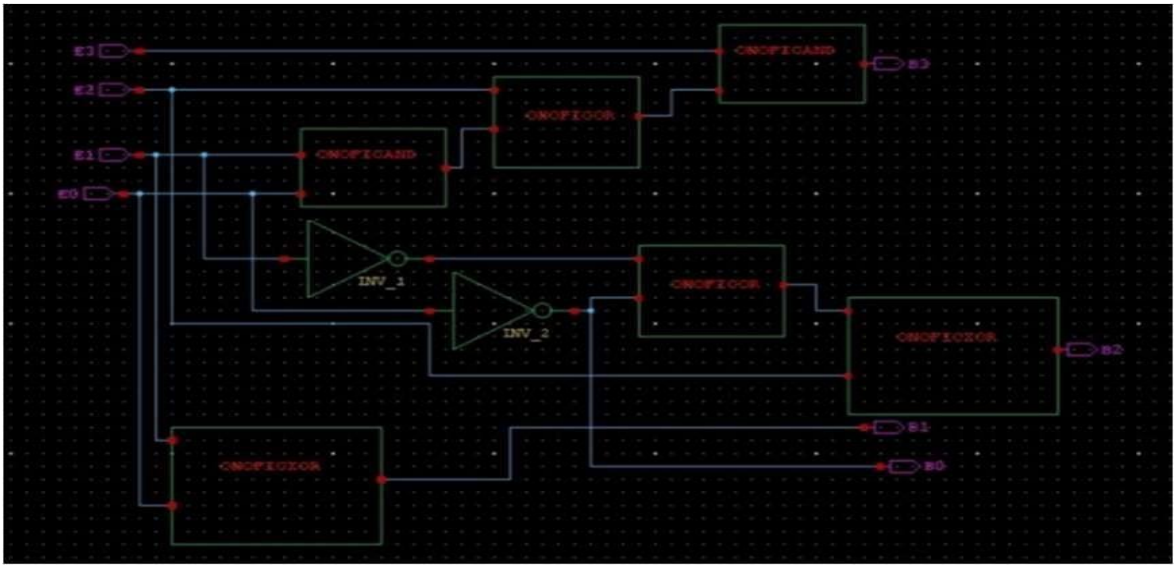

Fig.12. ONOFIC code converter

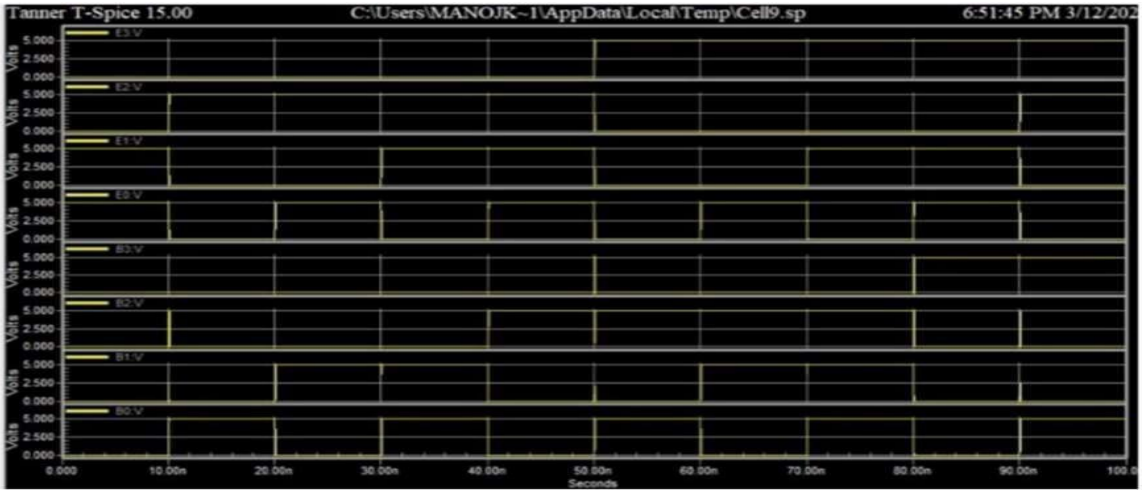

Fig.13. Stack ONOFIC code converter waveform

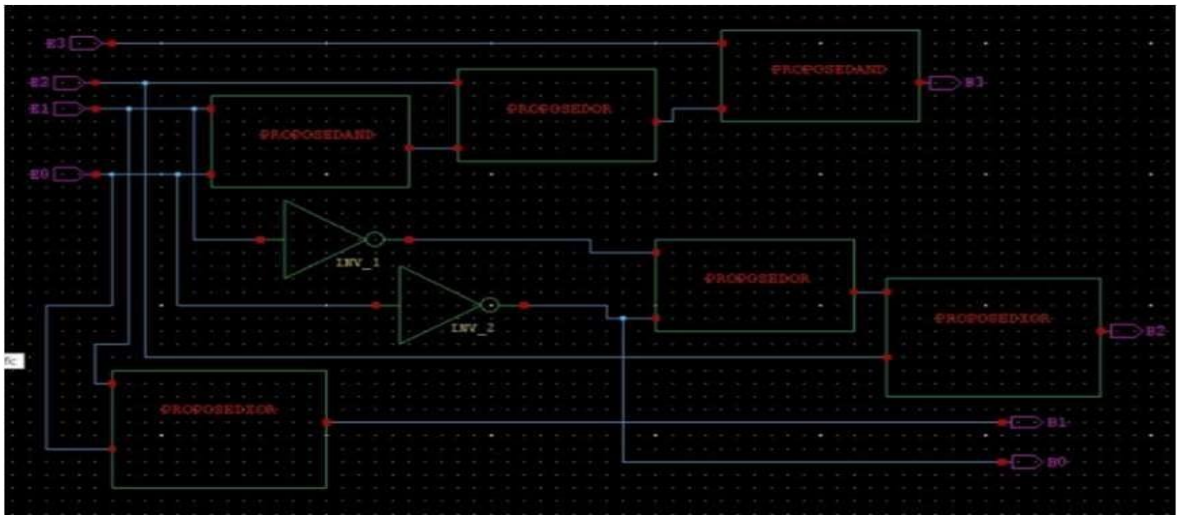

Fig.14. Alternate ONOFIC code converter

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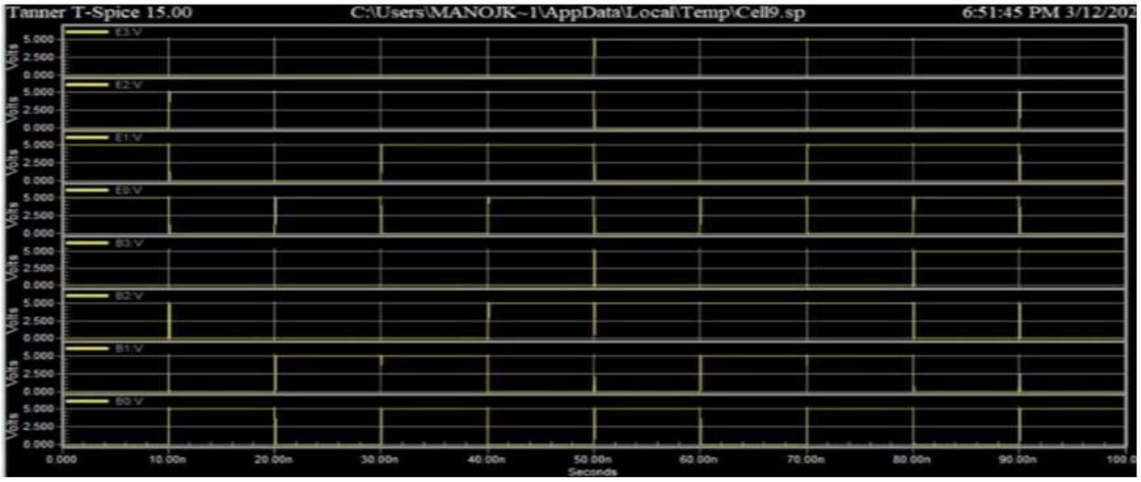

Fig.15. Alternate ONOFIC code converter waveform

Table.3.

Voltage	Proposed ONOFIC technique	Stack ONOFIC technique	ONOFIC technique
5V	0.126 µW	0.14675 µW	0.19225 µW
2.5V	0.1039 µW	0.2289 µW	0.1188 µW
1.5V	0.0300 µW	0.0755 µW	0.0419 µW

Table-3 Explains the Comparison of average power consumption in ONOFIC, Stack ONOFIC and Alternative ONOFIC techniques for code converter

6. CONCLUSION

This work focuses on reducing power dissipation in CMOS circuits, targeting lower energy consumption and improved performance for integrated circuits (ICs) and electronic devices. The Alternative ONOFIC method is proposed as a solution, aim ng to be suitable for circuit design using the EDA Tanner tool. It demonstrably reduces power consumption compared to other techniques like ONOFIC and Stack ONOFIC .Results from circuit simulations show that Alternative ONOFIC offers the greatest power reduction. This, combined with insights gained from various CMOS analysis methods and design techniques, paves the way for potentially improving both power efficiency and speed in future circuit designs.

7. FUTURE SCOPE

Deep Alternative ONOFIC understanding, optimize performance, and develop design methodology. Expand applicability to different transistor technologies and circuit types. Integrate with emerging technologies like power management and 3D integration. Develop automated design tools, explore performance-power trade-offs, and address reliability.

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